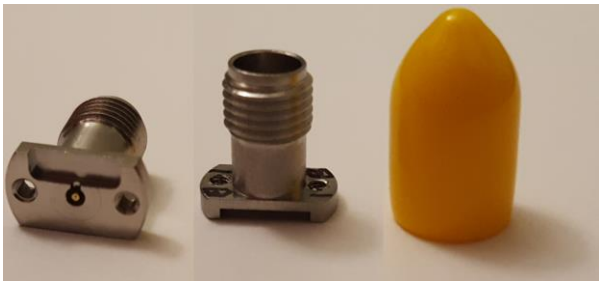
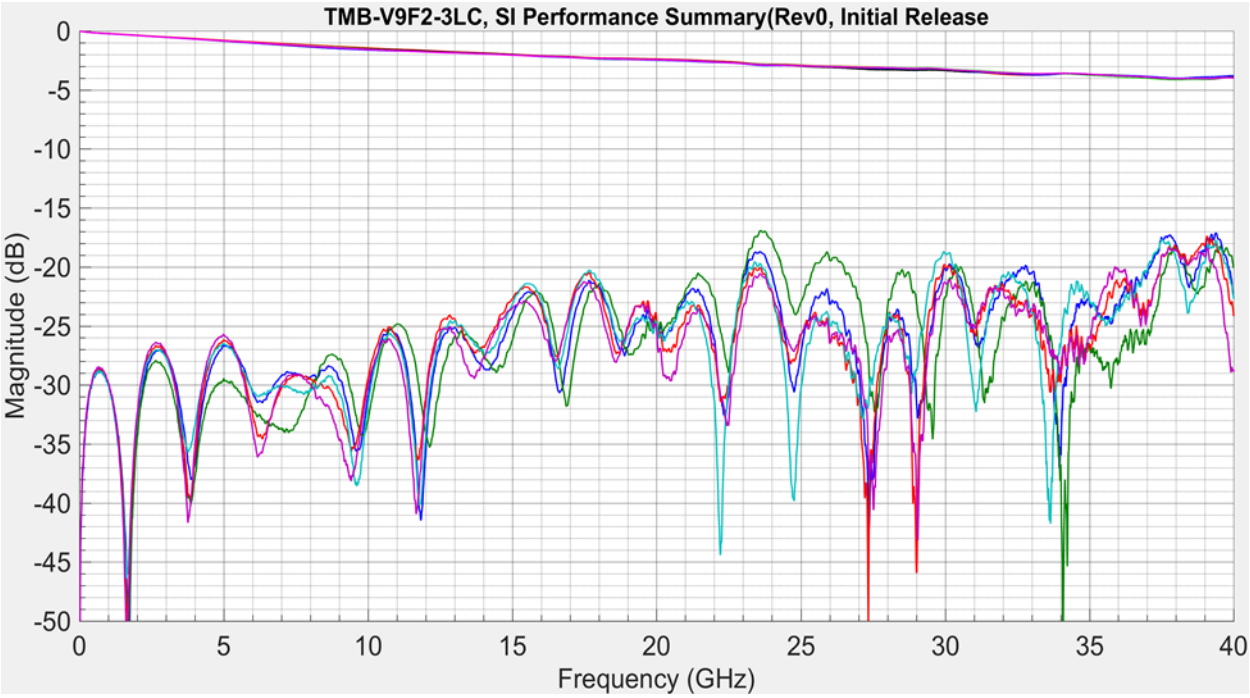
SIGNAL INTEGRITY REPORT

Test and Measurement Performance Report

Part Number TMB-V9F2-3LC
(2.92 mm Vertical Launch CPW Solderless Precision Connector)
Distribution: *Internal & External Use*



SI Performance Summary
(Attenuation & Reflections, Single-Ended)



* 10 connectors are shown, measured in pairs. (5 measurements) For further details regarding testing setup, configurations please see the rest of the report.

REVISION:	ECN INFORMATION:	TITLE:	SHEET No.
1	EC No: **N/A** DATE: **04/ 21 / 2020**	**2.92 mm Vertical Launch CPW Solderless Precision Connector (TMB-V9F2-3LC)**	**1** of **8**

DOCUMENT NUMBER:	SI ENGINEER:	DESIGN ENGINEER	ENGINEERING MANAGER
RSI- TMB_V9F2_3LC	**R.Stavoli**	**P. Volkov**	**E.Soubh**

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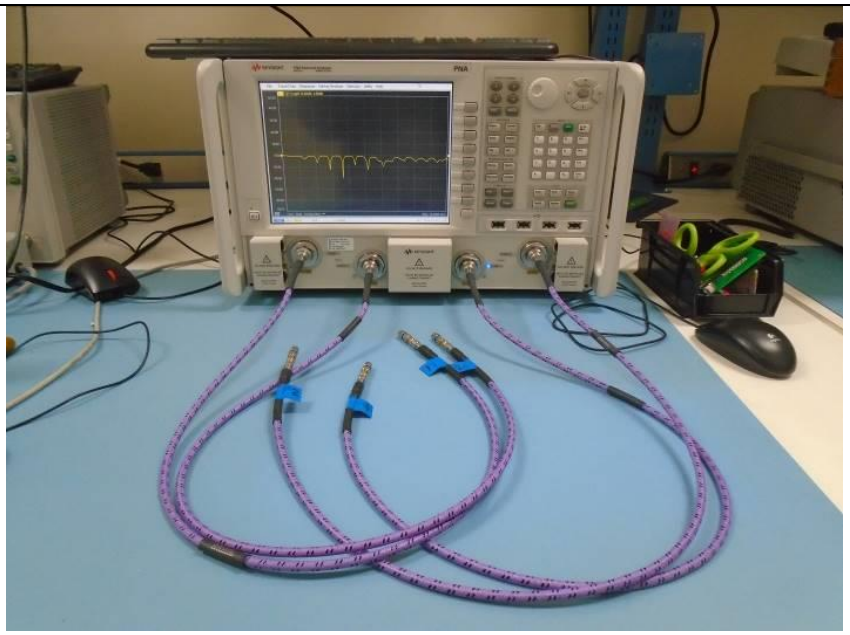
1.0 TEST SETUP AND DUT

Equipment, fixtures, and methods

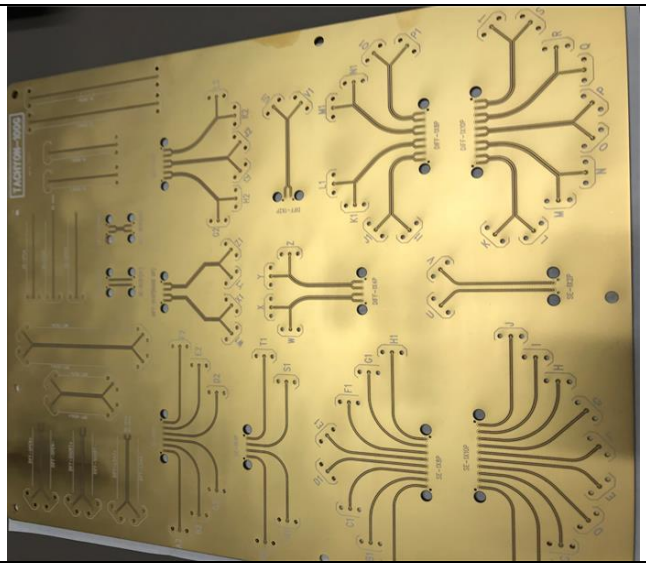
Test method: All data measured from test PCB shown below and a N5227A PNA Network Analyzer

- Calibration was performed up to the 2. 92mm adapters using calibration kit: 8770F
- Data was swept from 10 MHz to 40GHz for 4000 points
- Data averaging was turned off.
- Data is not dembedded and includes the board trace/transition and two RF vertical launch CPW precision connectors



Assembly Description

- T&M PN: TMB-V9F2-3LC
- Carlisle DUT PCB: Core HC 2.5mm CPW Test Board (Rev D0)
- **Measured on: 1x Cal Trace (SE-1xCal+)**
- Port 1: 2.92mm vertical mount CPW
- Port 2: 2.92mm vertical mount CPW



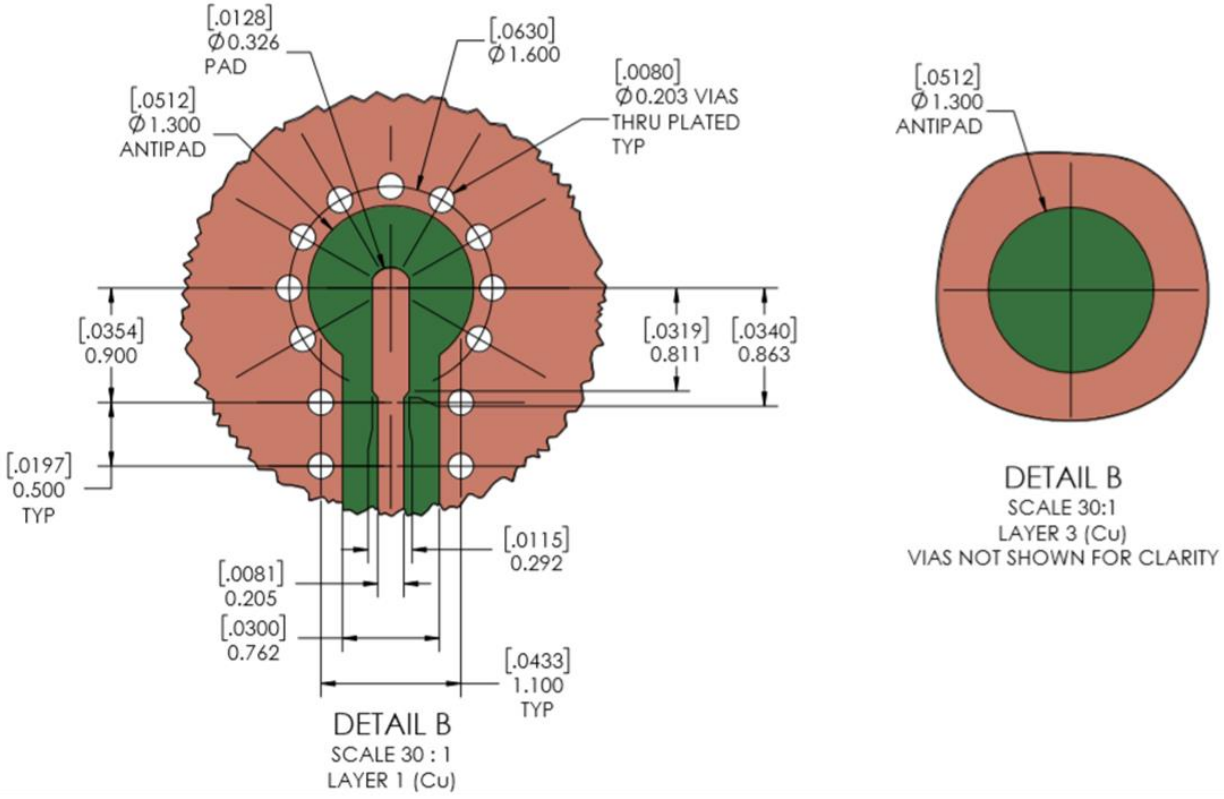
Testing Samples:

- 10 Samples
- 5 Channels
- 5 THRU Measurements (5 Channels = 10 samples) -> -Single-Ended

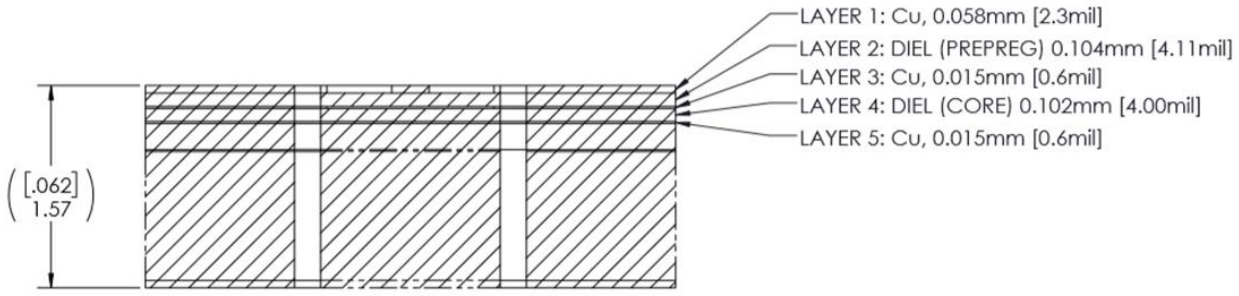
2.0 BOARD DETAILS & STACKUP

- Carlisle Core HC 2.5mm CPW Test Board
  - Revision D, Coplanar Waveguide
  - **Interconnects placed on 1x Cal Traces**
- Dielectric Material: Tachyon 100G (Dk.2.97, Df 0.0014 @ 20 Ghz)
  - Thickness: 0.104mm / 4.11 mil

TMB-V9F2-3LC, Interconnect Footprint



Core HC 2.5mm CPW Test Board Stackup (RevD0)



C) **PCB FINISH**

1. **Surface Protective Plating**

   a. All exposed copper on the outer layers shall be plated with a protective surface finish.
   b. All exposed pads, edge fingers and plated through holes shall be ENIG with thickness listed in Table 2.

Table 2: Protective Plating Thickness

Nickel		Immersion Gold	
µm (microinch)		µm (microinch)	
Min.	Max.	Min.	Max.
2.5 (100)	13(512)	0.051 (2)	0.2032 (8)

2. **Solder Mask**

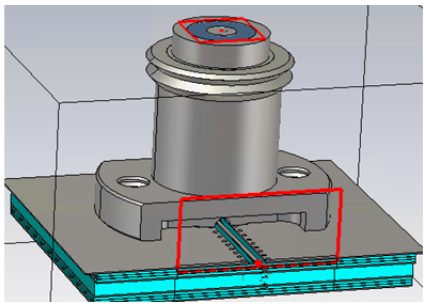
Apply an LPI solder mask to both sides of the board, the solder mask color is defined in the table.

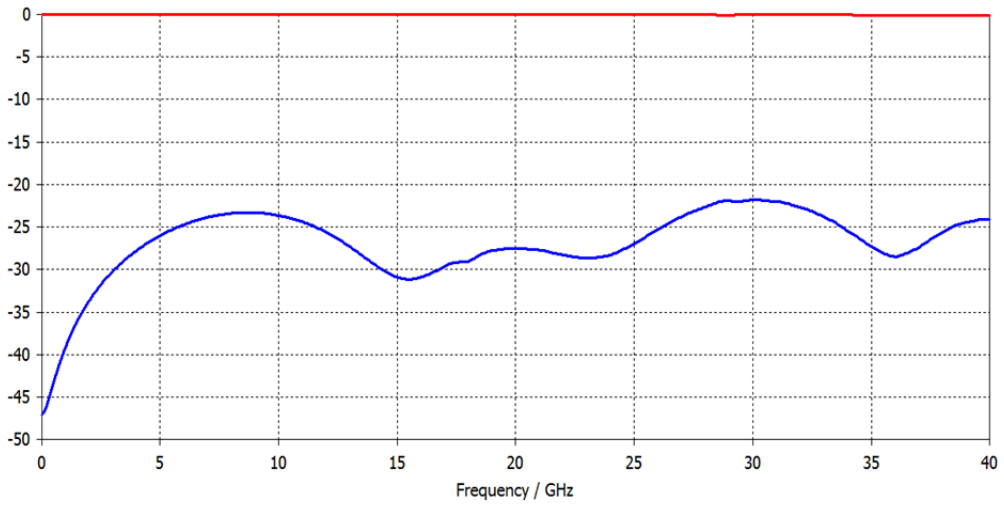
PCB PN	Soldermask color
NA	Green

3. **Silkscreen**

Silkscreen shall be permanent, non-conductive ink. There shall be no silkscreen on any solderable component pad.
Color: White

Simulated Data
1 connector to PCB





3.0 MEASUREMENT SET-UP

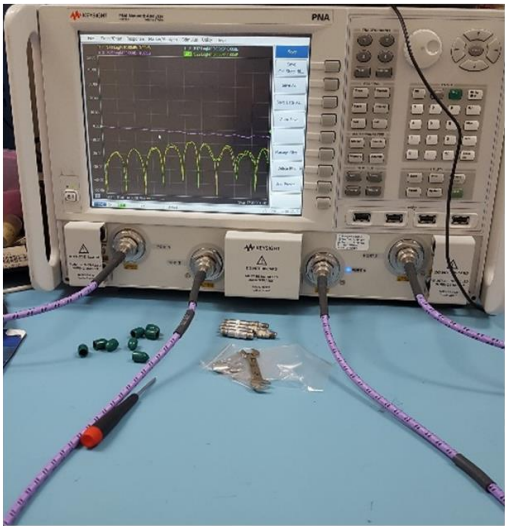
Port 1:
TMB-V9F2-3LC 2.92mm
Vertical Launch CPW
Solderless Precision
Connector # 1 A

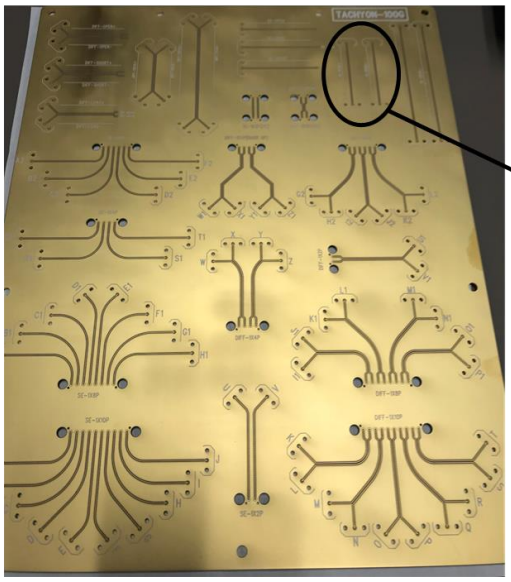
→

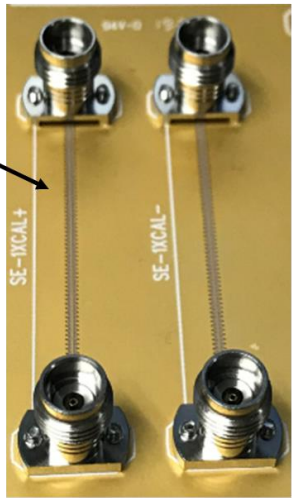
1x Cal Trace (SE-1XCal+)
Core HC 2.5mm CPW
Test Board (RevD0)

→

Port 2:
TMB-V9F2-3LC 2.92mm
Vertical Launch CPW
Solderless Precision
Connector # 1 B







Measurements are not dembedded and include the two 2.92mm vertical launch CPW solderless precision connectors, and the PCB (transition, traces)

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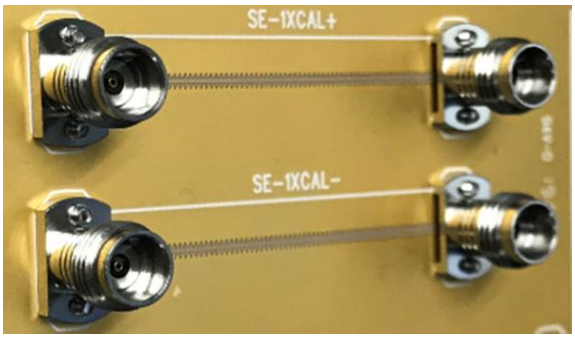
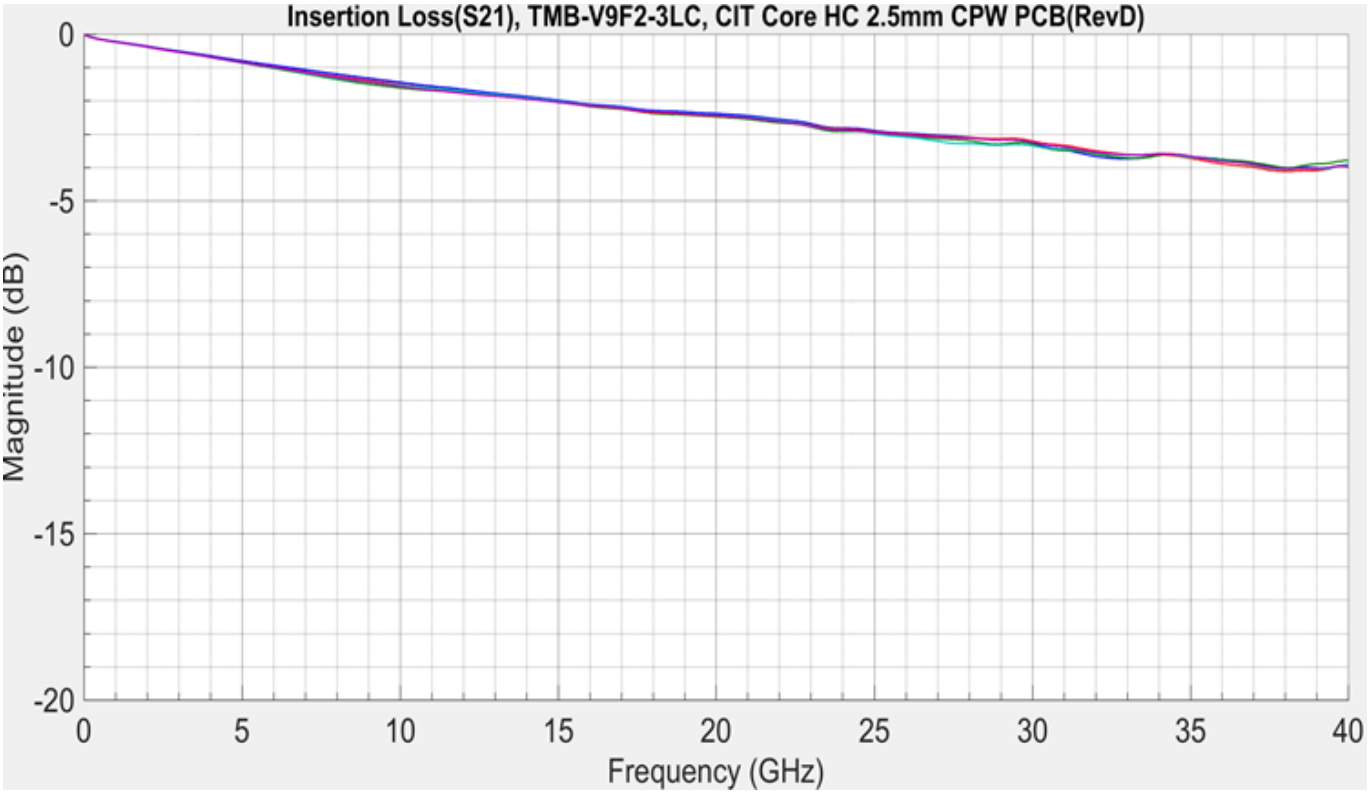
4.0 SIGNAL INTEGRITY RESULTS (CIT: CORE HC 2.5MM CPW PCB, 1X CAL TRACE)



Insertion Loss (S21), 10 connectors measured, 5 measurements



TMB-V9F2-3LC_292_CPW_1xCalPlus_HC2RevD0_P1C1A_P2C1B	3/25/2020 5:00 PM	S2P File	426 KB
TMB-V9F2-3LC_292_CPW_1xCalPlus_HC2RevD0_P1C2A_P2C2B	3/25/2020 5:03 PM	S2P File	426 KB
TMB-V9F2-3LC_292_CPW_1xCalPlus_HC2RevD0_P1C3A_P2C3B	3/25/2020 5:05 PM	S2P File	426 KB
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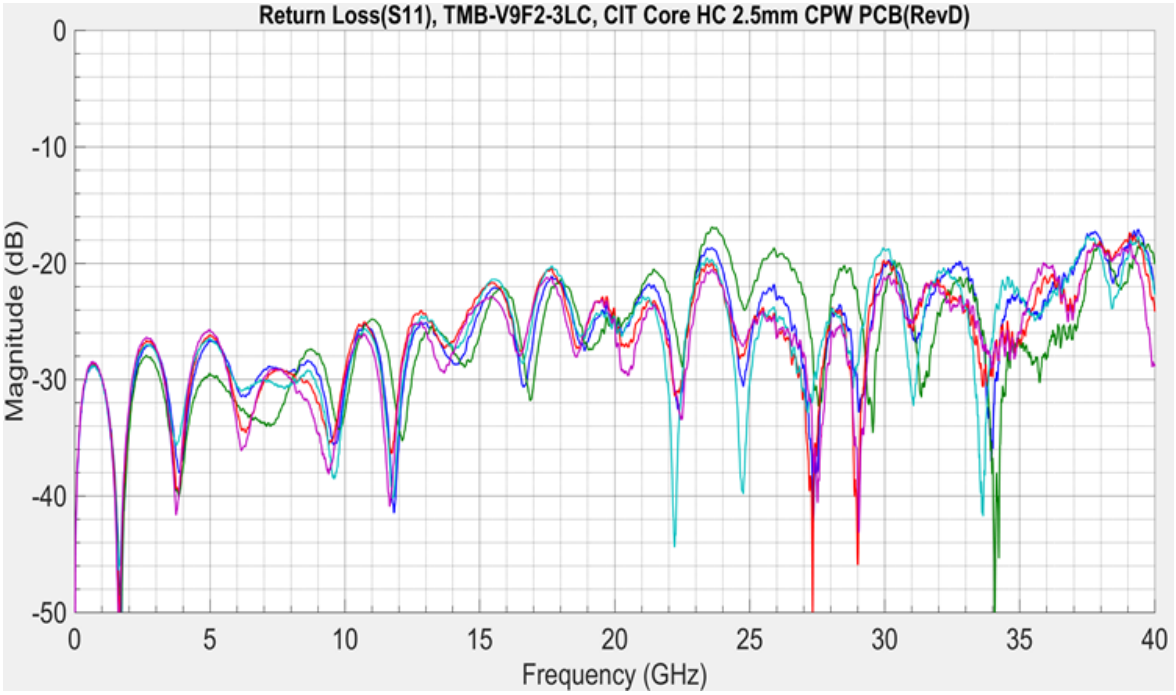
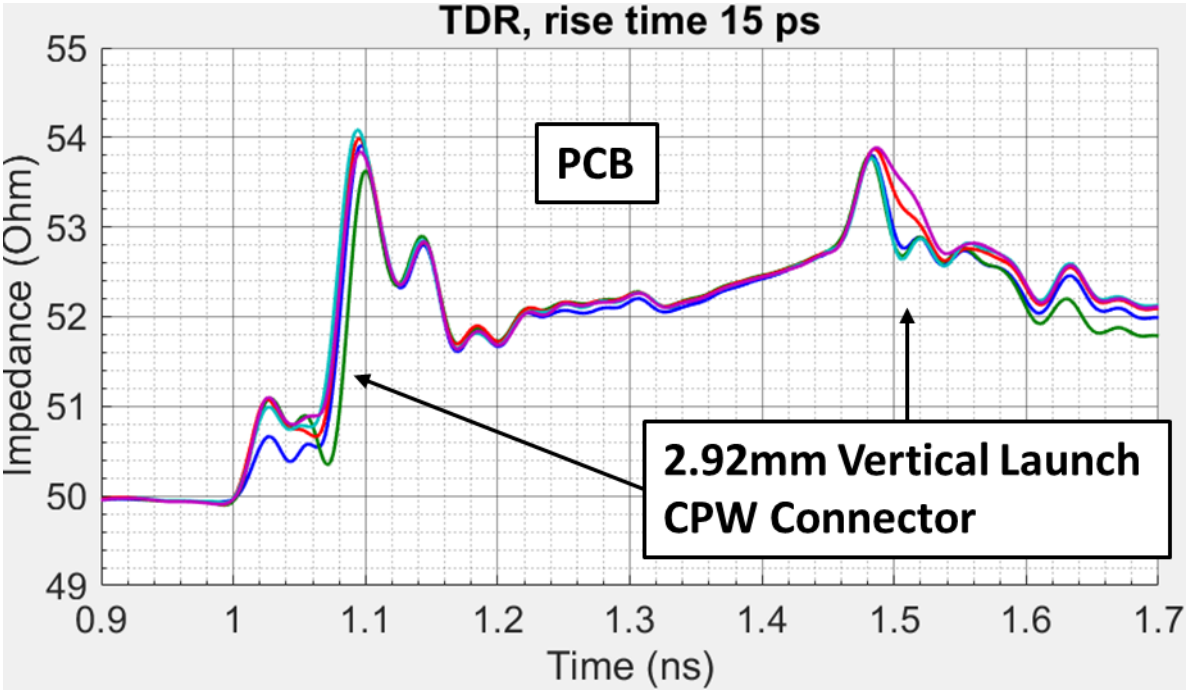
TMB-V9F2-3LC_292_CPW_1xCalPlus_HC2RevD0_P1C5A_P2C5B	3/25/2020 5:10 PM	S2P File	427 KB

SIGNAL INTEGRITY REPORT

Return Loss (S11), 10 connectors measured, 5 measurements





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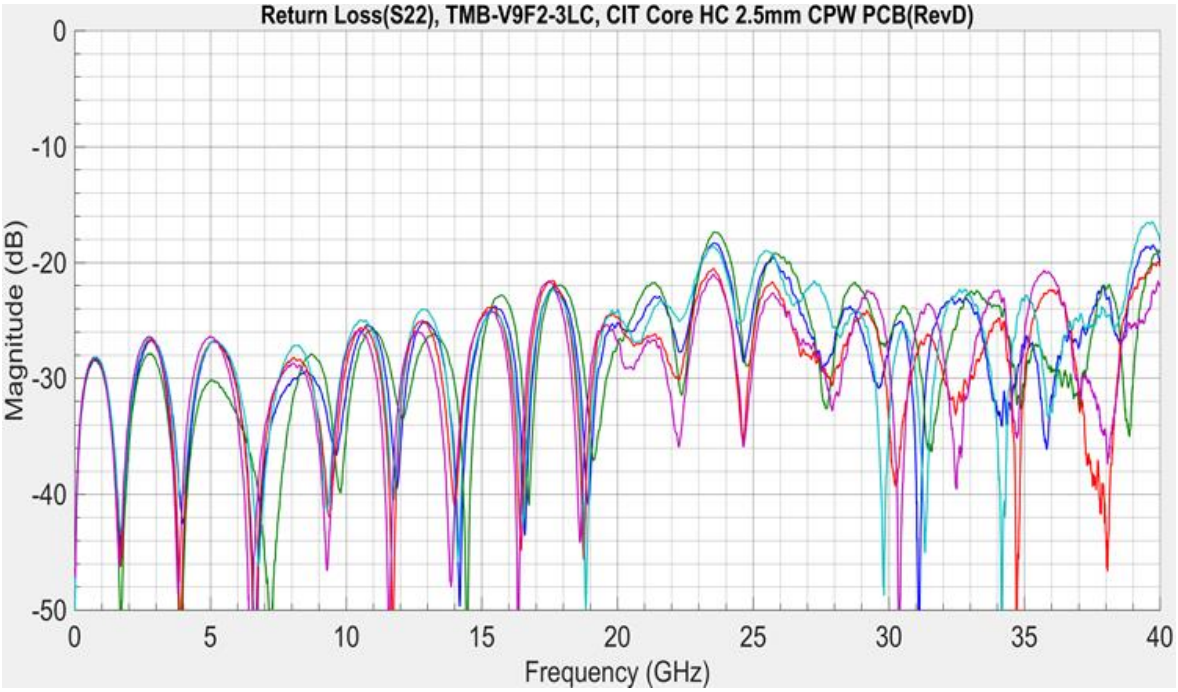
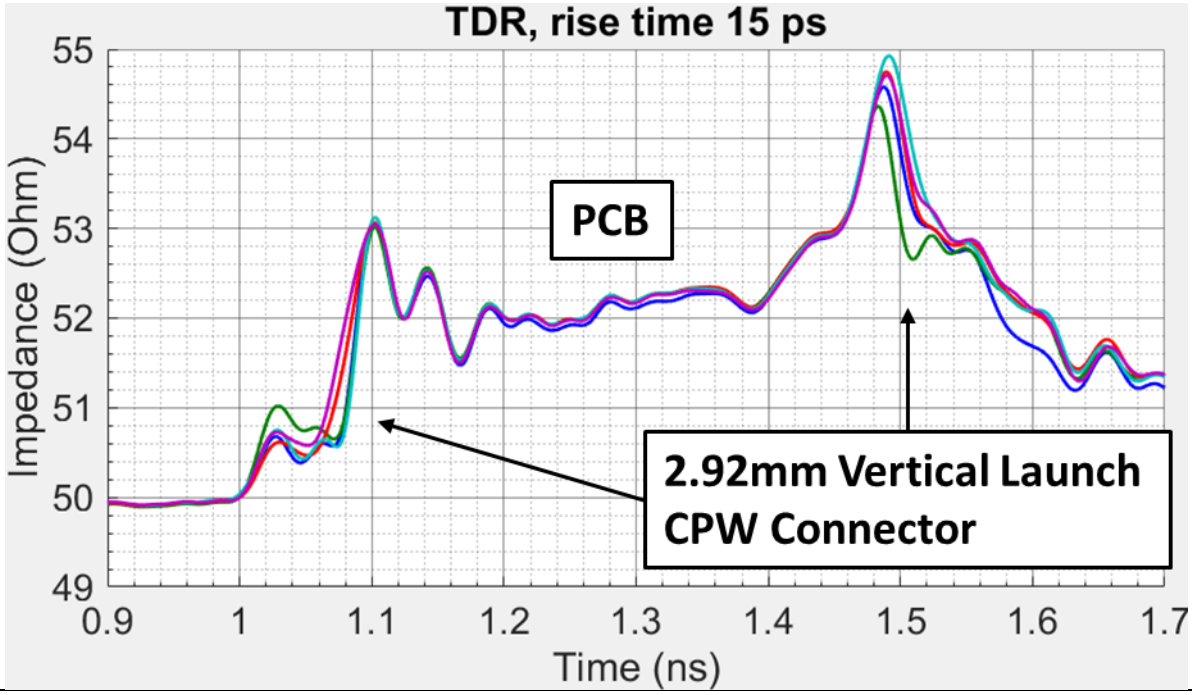
SIGNAL INTEGRITY REPORT

Return Loss (S22), 10 connectors measured, 5 measurements





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