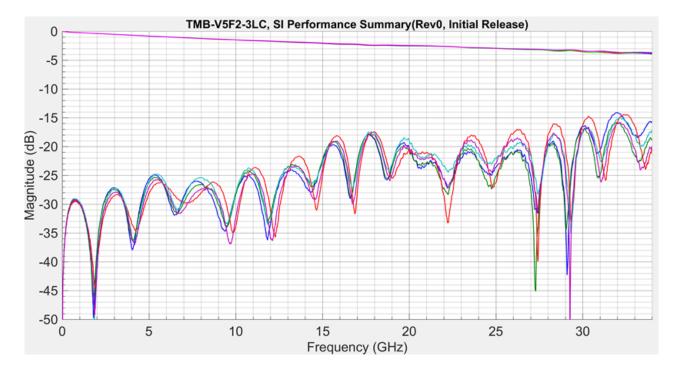


Test and Measurement Performance Report

Part Number TMB-V5F2-3LC (3.5 mm Vertical Launch CPW Solderless Precision Connector) **Distribution**: *Internal & External Use*



SI Performance Summary (Attenuation & Reflections, Single-Ended)



* 10 connectors are shown, measured in pairs. (5 measurements) For further details regarding testing setup, configurations please see the rest of the report.

| REVISION: | ECN INFORMATION: | TITLE: 3.5 mm Vertical Launch CPW | | | SHEET No. |
|-------------------|---------------------|-----------------------------------|-------------------|----------------------|----------------------|
| 1 | EC No: N/A | Solderless P | recision Connecto | or | 1 of 8 |
| • | DATE: 04/ 21 / 2020 | (TMB-V5F2-3 | 1010 | | |
| DOCUMENT NUMBER: | | SI ENGINEER: | DESIGN ENGINEER | ENGINEERING | MANAGER |
| RSI- TMB_V5F2_3LC | | R.Stavoli | P. Volkov E.Soubh | | bh |
| | | | TEMF | LATE FILENAME: SPM[S | SIZE_A](V.1).DOC |

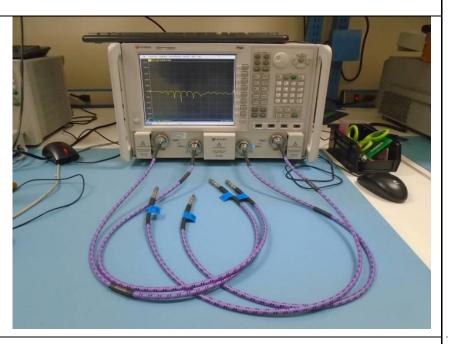


1.0 TEST SETUP AND DUT

Equipment, fixtures, and methods

Test method: All data measured from test PCB shown below and a N5227A PNA Network Analyzer

- Calibration was performed up to the
 2. 92mm adapters using calibration
 kit: 8770F
- Data was swept from 10 MHz to 34GHz for 3400 points
- Data averaging was turned off.
- Data is not dembedded and includes the board trace/transition and two RF vertical launch CPW precision connectors

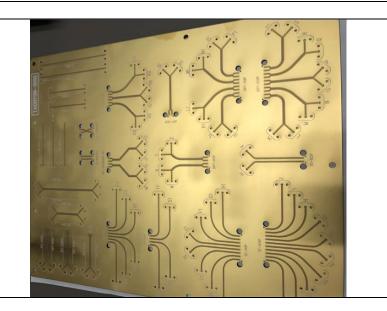


Assembly Description

- T&M PN: TMB-V5F2-3LC
- Carlisle DUT PCB: Core HC 2.5mm CPW Test Board (Rev D0)
- Measured on: 1x Cal Trace (SE-1xCal+)

•

- Port 1: 3.5mm vertical mount CPW
- Port 2: 3.5mm vertical mount CPW

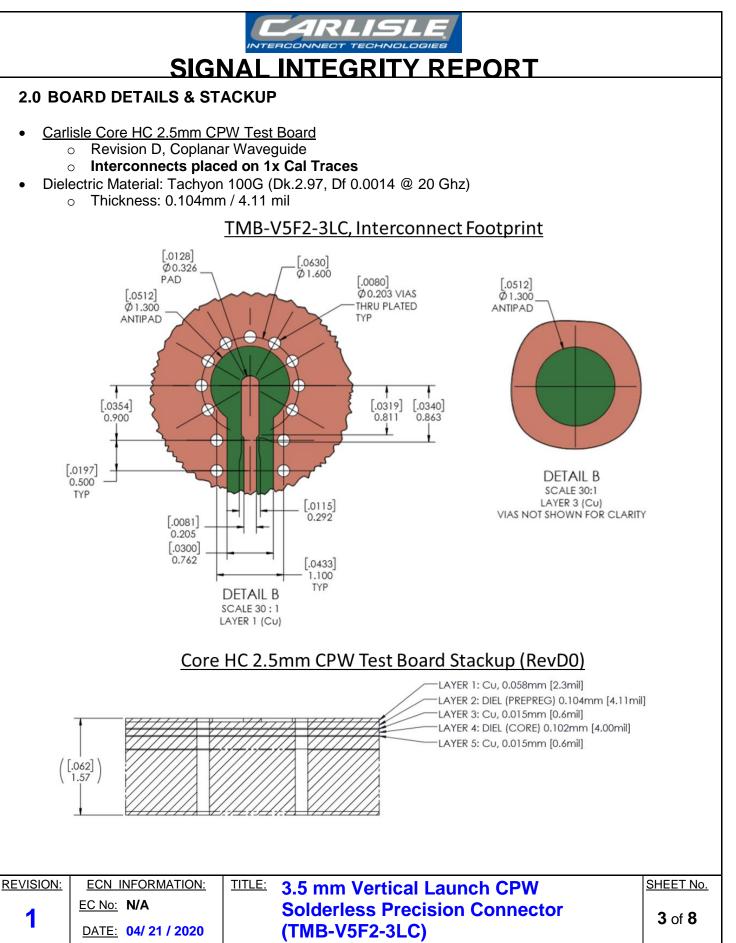


5 THRU Measurements (5 Channels = 10 samples) -> -Single-Ended

| Testing Samples: | |
|--------------------------------|---|
| 10 Samplas | Τ |

10 Samples5 Channels

| REVISION: | ECN INFORMATION: | TITLE: 3.5 mm Vertion | cal Launch CPW | | SHEET No. |
|---------------------------------|---------------------|--|-------------------|---------|----------------------|
| EC No: N/A | | Solderless Precision Connector | | | 2 of 8 |
| - | DATE: 04/ 21 / 2020 | (TMB-V5F2-3 | | | |
| DOCUMENT NUMBER: | | SI ENGINEER: DESIGN ENGINEER ENGINEERING | | MANAGER | |
| RSI- TMB_V5F2_3LC | | R.Stavoli | P. Volkov E.Soubh | | bh |
| TEMPLATE FILENAME: SPM[SIZE_A](| | | SIZE_A](V.1).DOC | | |



| | | | / | |
|------------------|--|---------------------|--|---------------------|
| DOCUMENT NUMBER: | | <u>SI ENGINEER:</u> | DESIGN ENGINEER | ENGINEERING MANAGER |
| RSI-TMB_V5F2_3LC | | R.Stavoli | P. Volkov | E.Soubh |
| | | | TEMPLATE FILENAME: SPM[SIZE_A](V.1).DO | |



SIGNAL INTEGRITY REPORT

C) PCB FINISH

1. Surface Protective Plating

- a. All exposed copper on the outer layers shall be plated with a protective surface finish.
- b. All exposed pads, edge fingers and plated through holes shall be ENIG with thickness listed in Table 2.
 - Table 2: Protective Plating Thickness

| Nickel | | Immersion Gold | | |
|----------------|---------|----------------|------------|--|
| µm (microinch) | | µm (microinch) | | |
| Min. | Max. | Min. Max. | | |
| 2.5 (100) | 13(512) | 0.051 (2) | 0.2032 (8) | |

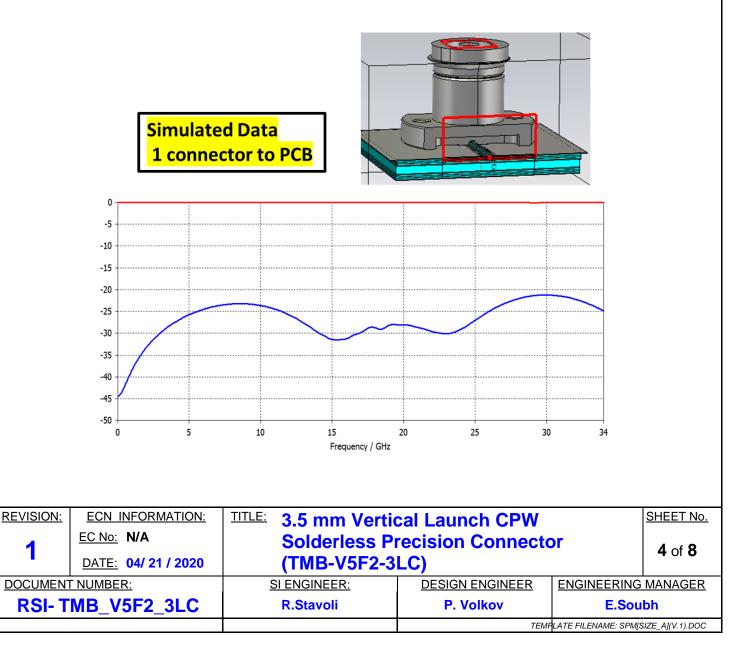
2. Solder Mask

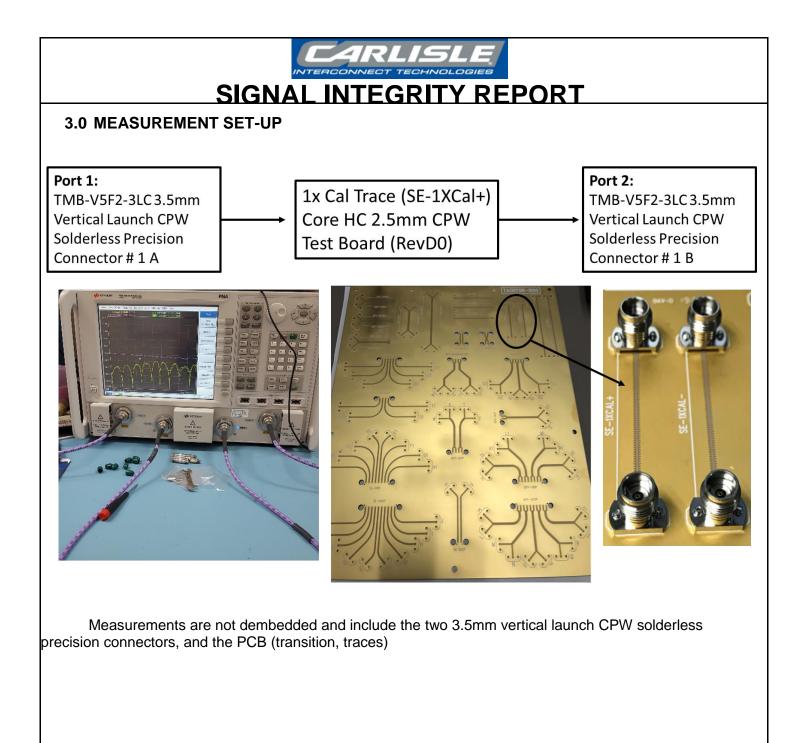
Apply an LPI solder mask to both sides of the board, the solder mask color is defined in the table.

| PCB PN | Soldermask color | |
|--------|------------------|--|
| NA | Green | |
| | | |

3. Silkscreen

Silkscreen shall be permanent, non-conductive ink. There shall be no silkscreen on any solderable component pad. Color: White





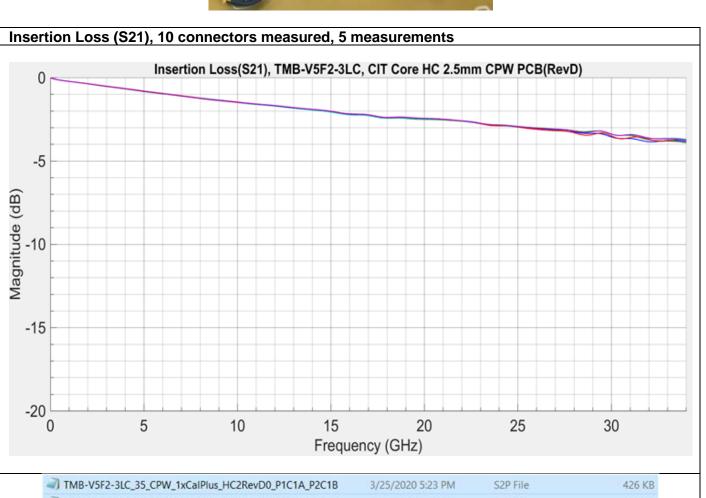
| REVISION: | ECN INFORMATION: | TITLE: 3.5 mm Verti | cal Launch CPW | | SHEET No. |
|-------------------|------------------------|---------------------|-------------------|-------------|----------------------|
| 1 | EC No: N/A | Solderless P | recision Connecto | or | 5 of 8 |
| | DATE: 04/ 21 / 2020 | (TMB-V5F2-3 | LC) | | 500 |
| DOCUMENT NUMBER: | | SI ENGINEER: | DESIGN ENGINEER | ENGINEERING | MANAGER |
| RSI- TMB_V5F2_3LC | | R.Stavoli | P. Volkov E.Soubh | | bh |
| | TEMPLATE FILENAME: SPN | | SIZE_A](V.1).DOC | | |



SIGNAL INTEGRITY REPORT

4.0 SIGNAL INTEGRITY RESULTS (CIT: CORE HC 2.5MM CPW PCB, 1X CAL TRACE)





| 3/25/2020 5:26 PM | S2P File | 426 KB |
|-------------------|--|---|
| 3/25/2020 5:28 PM | S2P File | 425 KB |
| 3/25/2020 5:30 PM | S2P File | 426 KB |
| 3/25/2020 5:33 PM | S2P File | 426 KB |
| | 3/25/2020 5:28 PM 3/25/2020 5:30 PM | 3/25/2020 5:28 PM S2P File 3/25/2020 5:30 PM S2P File |

| <u>REVISION:</u> | ECN INFORMATION: EC No: N/A DATE: 04/ 21 / 2020 | TITLE: 3.5 mm Vertical Launch CPW Solderless Precision Connector (TMB-V5F2-3LC) | | <u>SHEET No.</u> 6 of 8 | |
|-------------------|---|---|-----------------|-----------------------------------|------------------|
| DOCUMENT NUMBER: | | SI ENGINEER: | DESIGN ENGINEER | ENGINEERING | MANAGER |
| RSI- TMB_V5F2_3LC | | R.Stavoli | P. Volkov E.Sou | | bh |
| | | | TEMP | I ATE FILENAME [,] SPMIS | SIZE AI(V 1) DOC |

