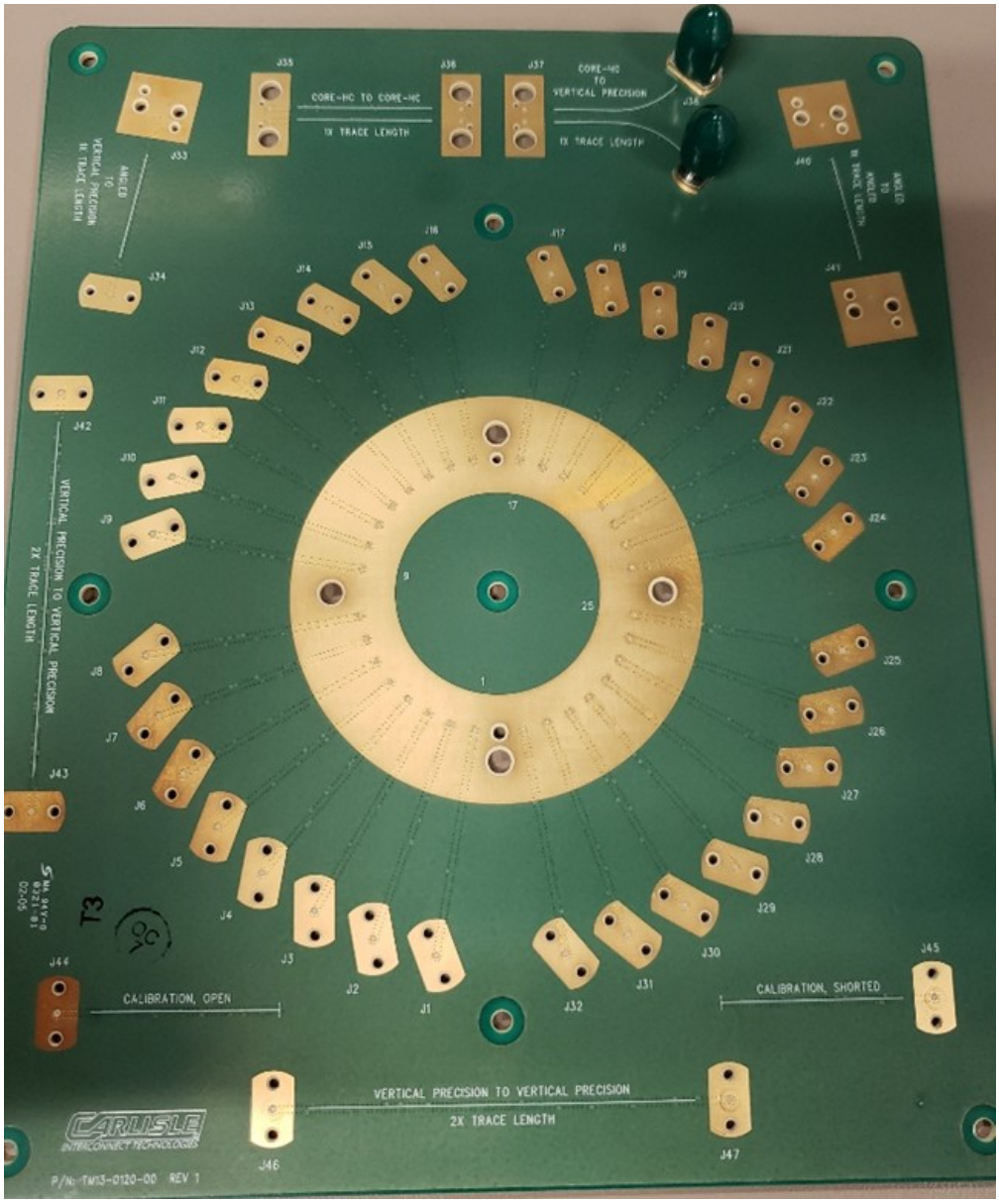
SIGNAL INTEGRITY REPORT

Test and Measurement Performance Report

Part Number TM7SSSH22S8MS028 (Core HC)
Distribution: Internal and External Use

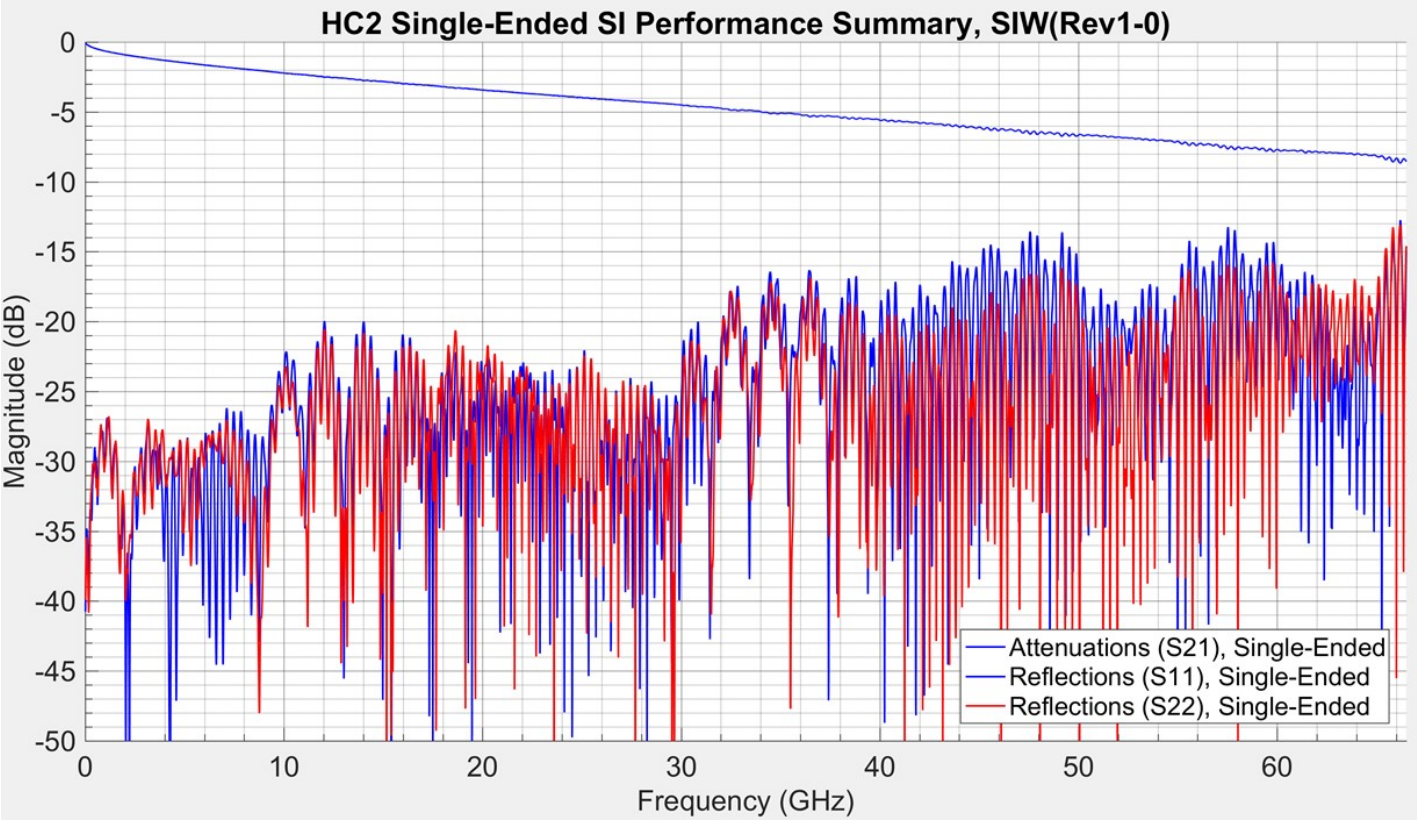


REVISION:	ECN INFORMATION:	TITLE:	SHEET No.
1	EC No: **N/A** DATE: **04/ 12 / 2021**	**Core HC 2.5mm SIW: Configuration 1X2P (HC2 to PCB)** **CARLISLE IT CONFIDENTIAL**	**1** of **21**

DOCUMENT NUMBER:	SI ENGINEER:	DESIGN ENGINEER	ENGINEERING MANAGER
RSI-TM7SSSH22S8MS028	**R.Stavoli**	**H.Tran**	**E.Soubh**

SIGNAL INTEGRITY REPORT

SI Performance Summary
(Attenuation & Reflections, Substrate Integrated Waveguide/SIW, Single-Ended)



* For further details regarding the testing setup and configuration please see the rest of the report.

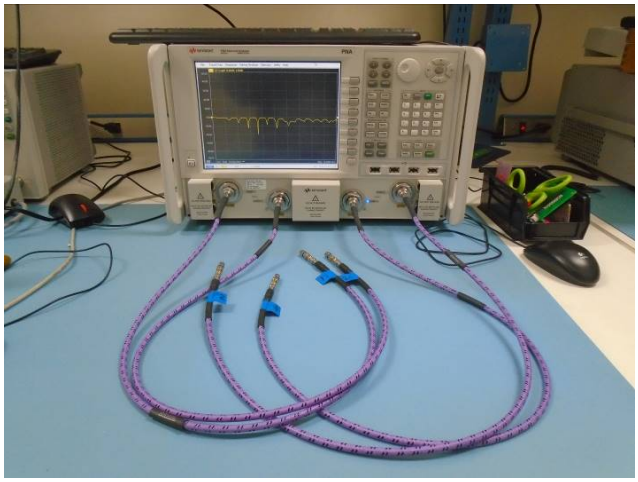
SIGNAL INTEGRITY REPORT

1.0 TEST SETUP AND DUT

Equipment, fixtures, and methods

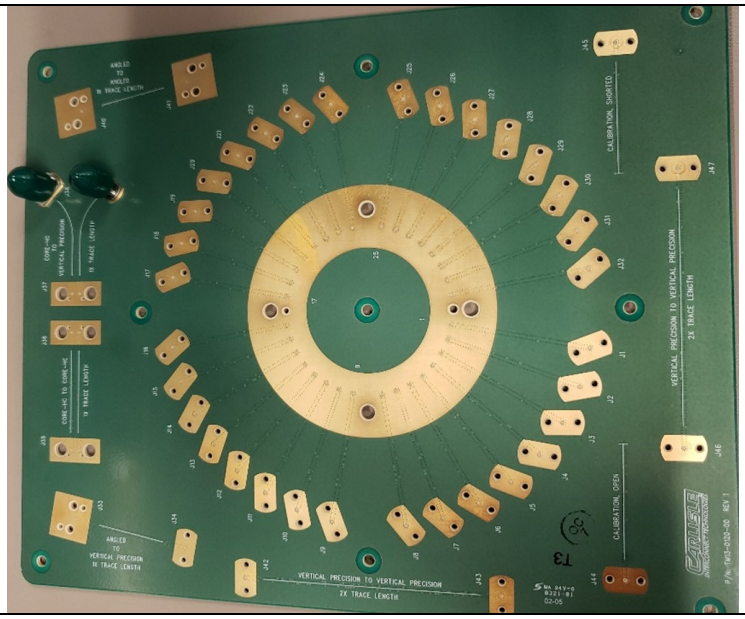
Test method: All data measured from test PCB shown below and a N5227A PNA Network Analyzer

- Calibration was performed up to the 1. 85mm SMA adapters using calibration kit: 85058B
- Data was swept from 10 MHz to 67GHz for 6700 points
- Data averaging was turned off.
- Data is not dembedded and includes the board traces and the Core HC cable assembly



Assembly Description

- T&M PN: TM7SSSH22S8MS028
- 2- Position LCP Connector Housing, two pieces at the interface
- **11-inch solid center conductor 092 coax cable**
- Carlisle DUT PCB: TM13-0120-00
  Core HC 32-position eval board, SIW, Vertical Launch, **Rev 1, #0**
- Port 1: 1.85mm Cable Connector (Core HC)
- Port 2: 1.85mm Stripline Vertical Launch Precision Connector (on HC2, SIW PCB)

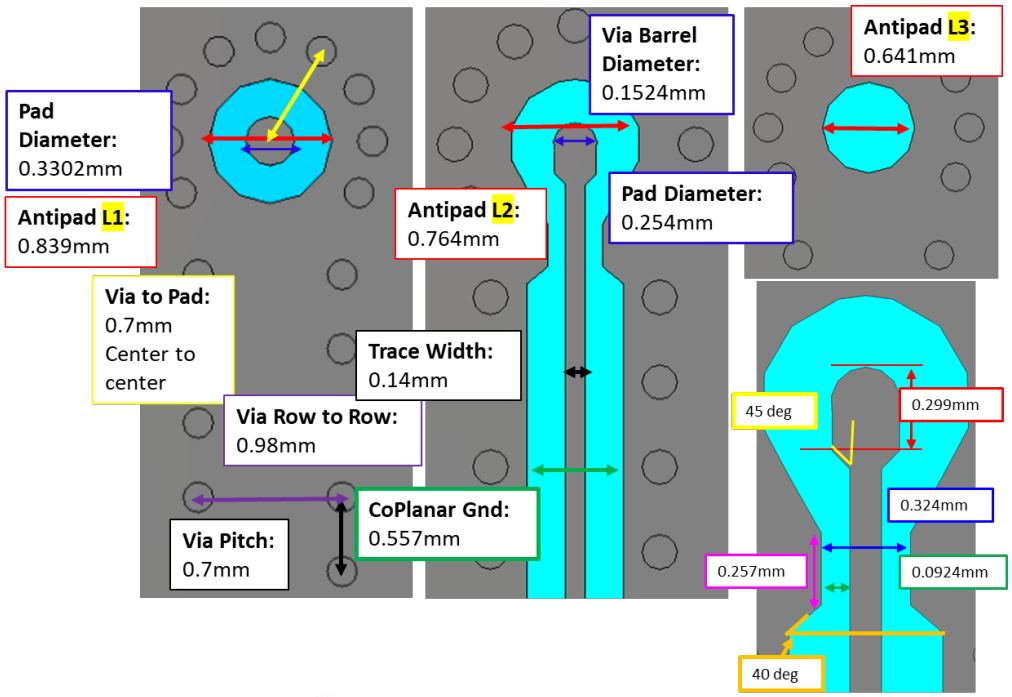


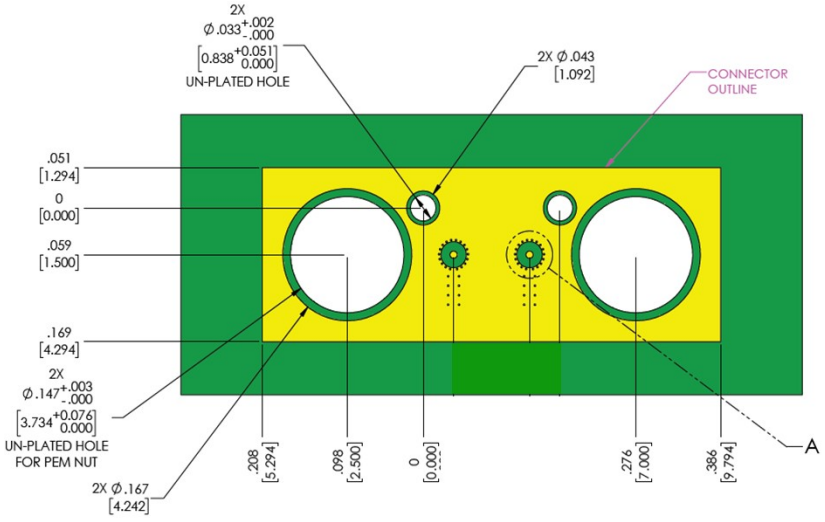
Testing Samples:

• 4 Samples • 4 Channels	• 2 THRU Measurements w/ PCB, Core HC2 → Core HC2 • 2 Crosstalk Meas. w/PCB (FEXT, NEXT), HC2 → HC2 • 1 THRU Measurements w/ PCB, HC2 → 1.85mm Vertical Precision Connector • 2 THRU Meas. w/RF Adaptor (2 Chan. x 1 samples)

2.0 BOARD STACKUP & FOOTPRINT INFORMATION

- TM13-0120-00 Carlisle Core HC 32-Position, SIW Test Board
  - Revision 1, #0, Substrate Integrated Waveguide(SIW), Vertical Launch
  - **Cable Assembly placed on 2-Position Single-Ended Footprint**
- Dielectric Material: Tachyon 100G (Dk.2.98, Df 0.0015 @ 20 GHz)
  - L1 Core Thickness: L1: 0.127mm / 5 mil
  - L2 PrePreg Thickness: L2: 0.149mm / 5.9mil
  -





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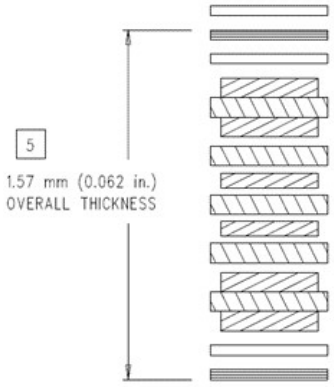
RSI-TM7SSSH22S8MS028	R.Stavoli	H.Tran	E.Soubh

6 LAYER BOARD
LAYER STACKUP DETAIL



3 12 4

LYR	NAME	TYPE	MATERIAL	THICKNESS	NOTES
		SILKSCREEN			
		SURFACE FINISH	ENIG		
		SOLDER MASK			0.02 mm (0.001 in) THICK
1	TOP	COPPER FOIL	VLP-2	0.041 mm (0.0016 in)	THICKNESS INCLUDES PLATING AND SURFACE FINISH
		CORE	TACHYON 100G	0.127 mm (0.0049 in)	Dk 2.98 / Df 0.0015
2	LAYER 2	COPPER FOIL	VLP-2	0.015 mm (0.0006 in)	1/2 oz.
		PREPREG	TACHYON 100G	0.147 mm (0.0058 in)	Dk 3.19 / Df 0.0021
3	LAYER 3	COPPER FOIL	VLP-2	0.015 mm (0.0006 in)	1/2 oz.
		PREPREG or CORE	TACHYON 100G	A/R TO MEET OVERALL THICKNESS	DIELECTRIC
4	LAYER 4	COPPER FOIL	VLP-2	0.015 mm (0.0006 in)	1/2 oz.
		PREPREG	TACHYON 100G	0.147 mm (0.0058 in)	Dk 3.19 / Df 0.0021
5	LAYER 5	COPPER FOIL	VLP-2	0.015 mm (0.0006 in)	1/2 oz.
		CORE	TACHYON 100G	0.127 mm (0.0049 in)	Dk 2.98 / Df 0.0015
6	BOTTOM	COPPER FOIL	VLP-2	0.041 mm (0.0016 in)	THICKNESS INCLUDES PLATING AND SURFACE FINISH
		SOLDER MASK			0.02 mm (0.001 in) THICK
		SURFACE FINISH	ENIG		

C) PCB FINISH

1. Surface Protective Plating

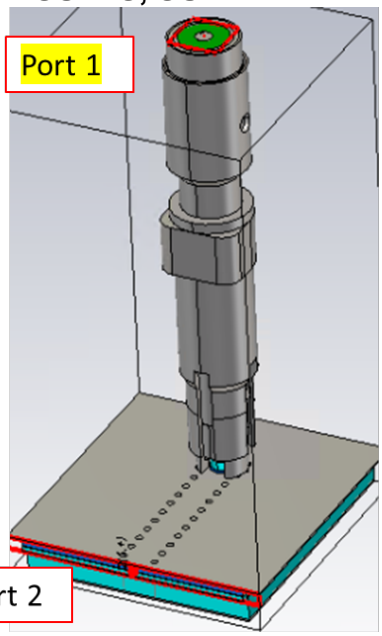
a. All exposed copper on the outer layers shall be plated with a protective surface finish.
b. All exposed pads, edge fingers and plated through holes shall be ENIG with thickness listed in Table 2.

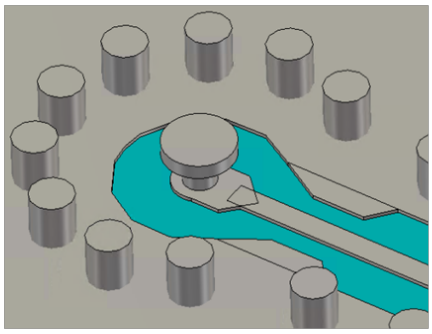
Table 2: Protective Plating Thickness

Nickel		**Immersion Gold**	
µm (microinch)		µm (microinch)	
Min.	Max.	Min.	Max.
2.5 (100)	13(512)	0.051 (2)	0.2032 (8)

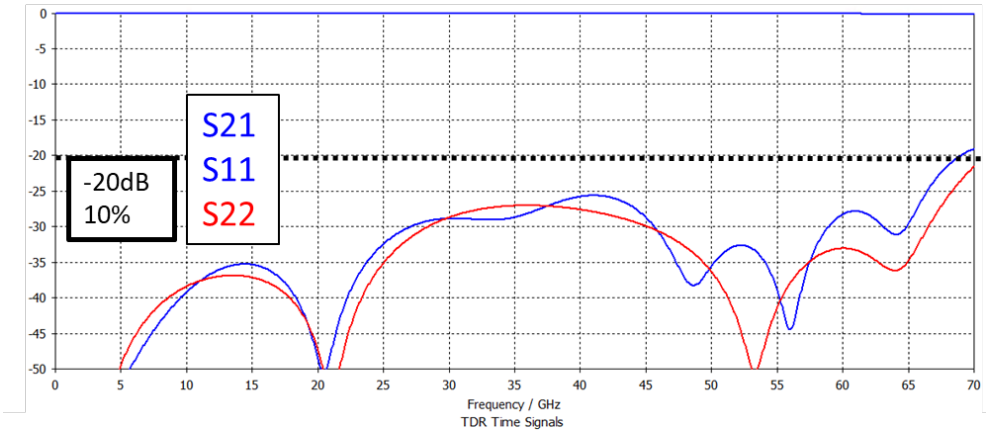
SIGNAL INTEGRITY REPORT

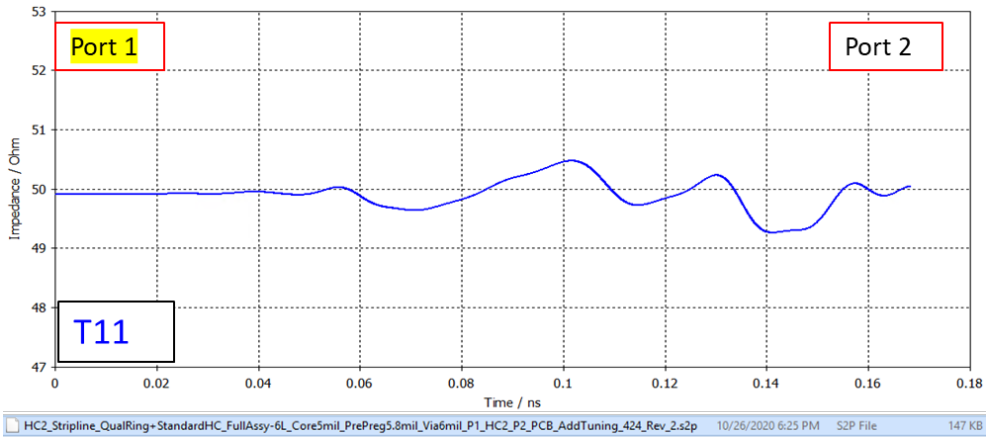
3.0 SIMULATION RESULTS, SUBRTRATE INTEGRATED WAVEGUIDE, SINGLE-ENDED





Diameter:
Signal Pad (L1): 0.3302mm/13mil
Antipad (L1): 0.839mm/33.07mil
Signal Pad (L2): 0.254mm /10mil
Finish Via: 0.1524mm/6mil





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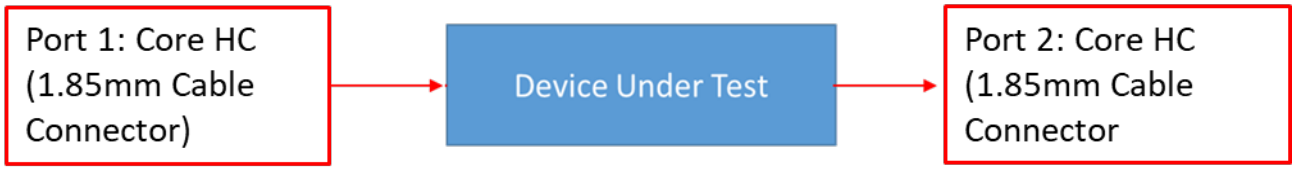
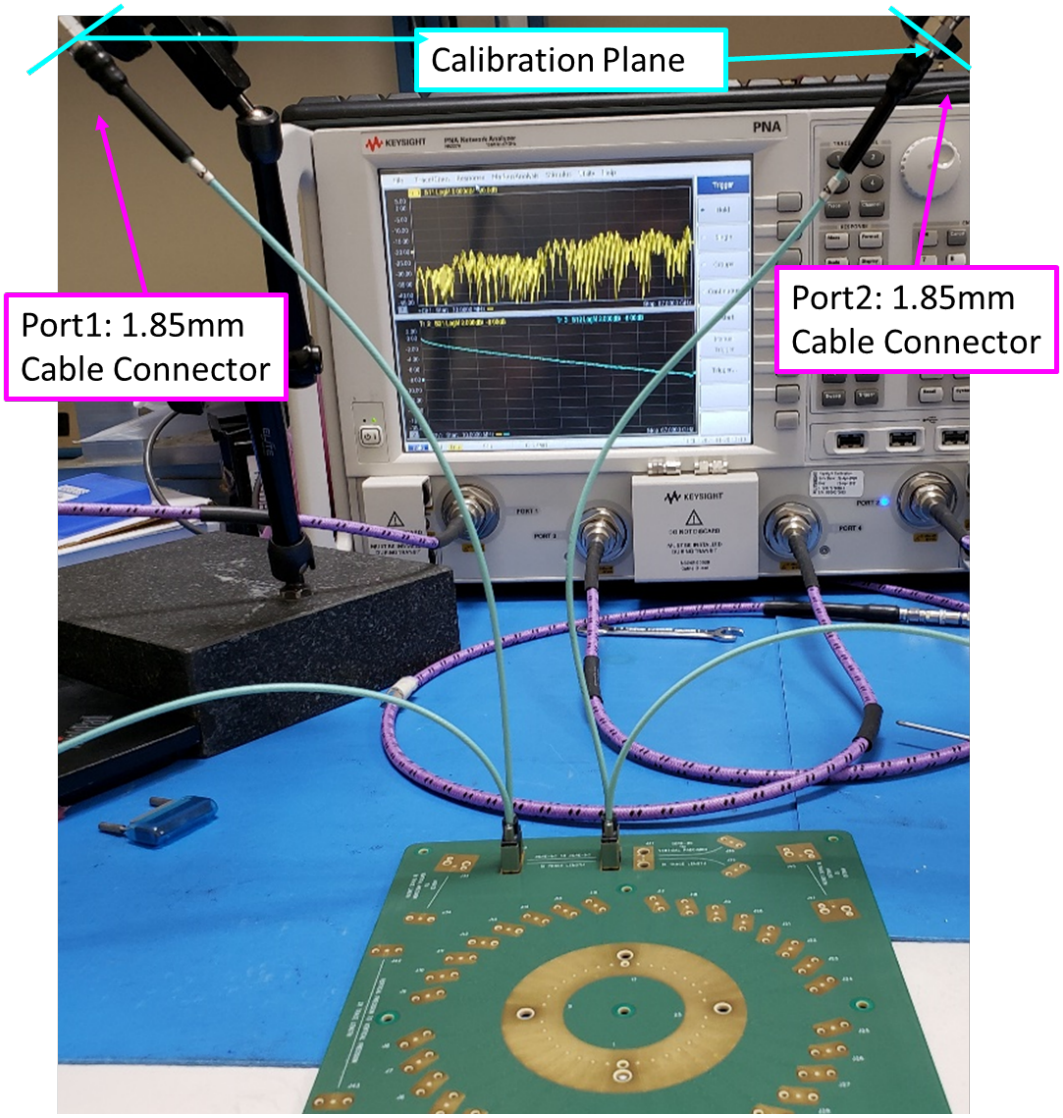
RSI-TM7SSSH22S8MS028	R.Stavoli	H.Tran	E.Soubh

SIGNAL INTEGRITY REPORT

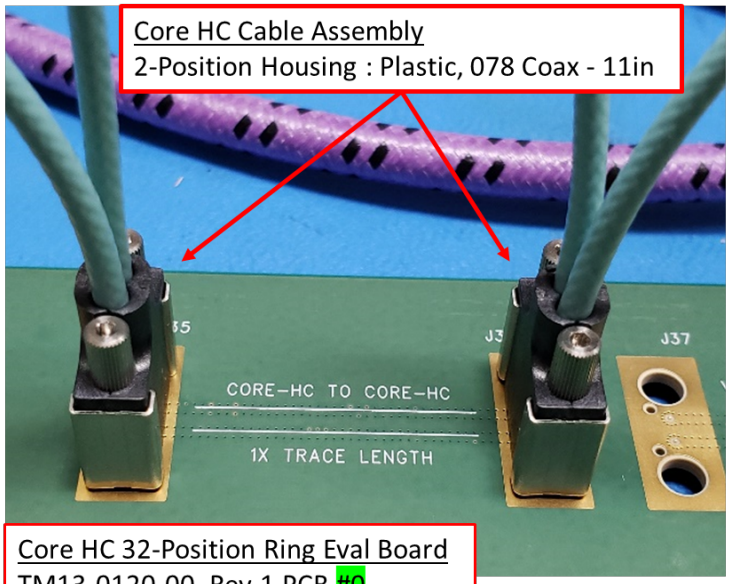
4.0 MEASUREMENT SET-UP, CORE HC2 → HC2, SINGLE-ENDED (HC2 SIW REV1 PCB)

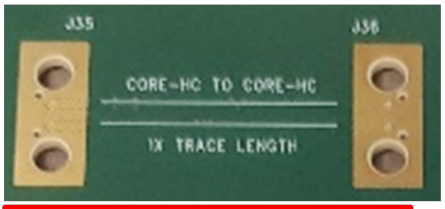


Measurements are not dembedded and include the **Core HC assemblies** (cable connector, cable, interconnect), PCB (transitions, traces)

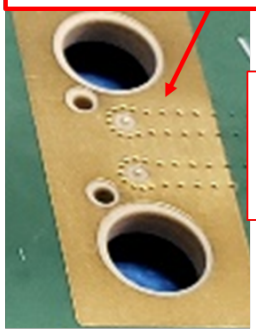


SIGNAL INTEGRITY REPORT





Core HC2 , 2-Position Footprint

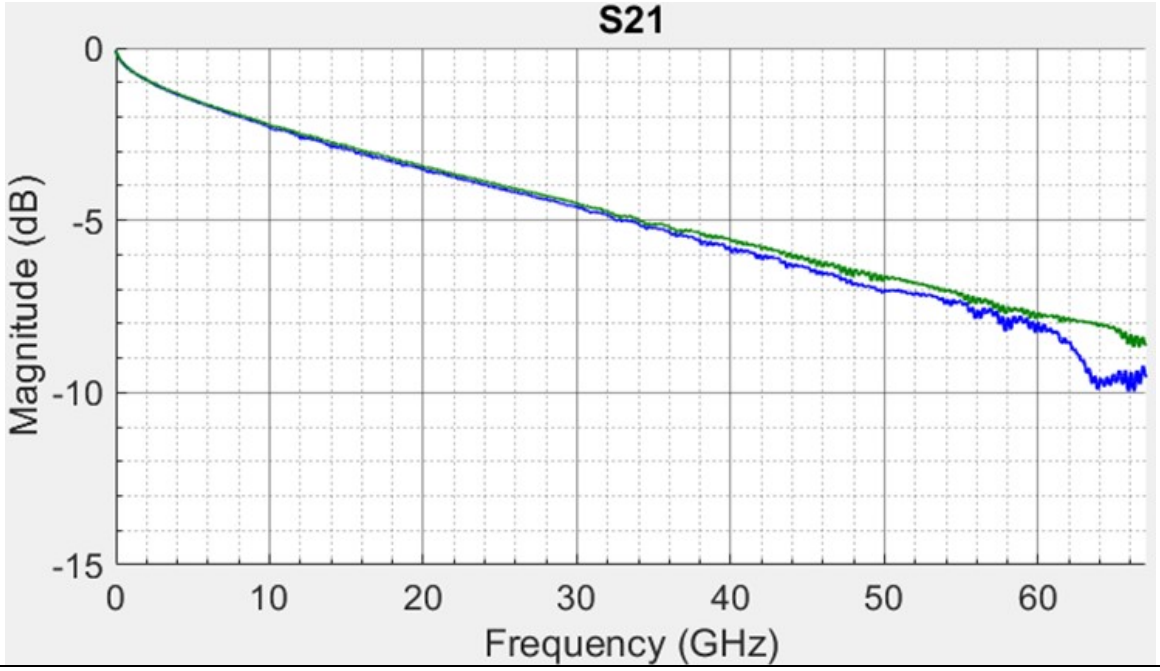


Pad Geometry:
Signal Pad Diam.(L1): 0.3302mm/13mil
Antipad Diam.(L1): 0.839mm/33.07mil
Signal Pad Diam.(L2): 0.254mm /10mil
Finish Via Diam: 0.1524mm/6mil

5.0 SIGNAL INTEGRITY RESULTS, SINGLE-ENDED (HC2 SIW REV1 BOARD)

Insertion Loss (S21), Single-Ended

(CoreHC Channels: 3→4 & 11 → 2, Board Locations: J35, J36)



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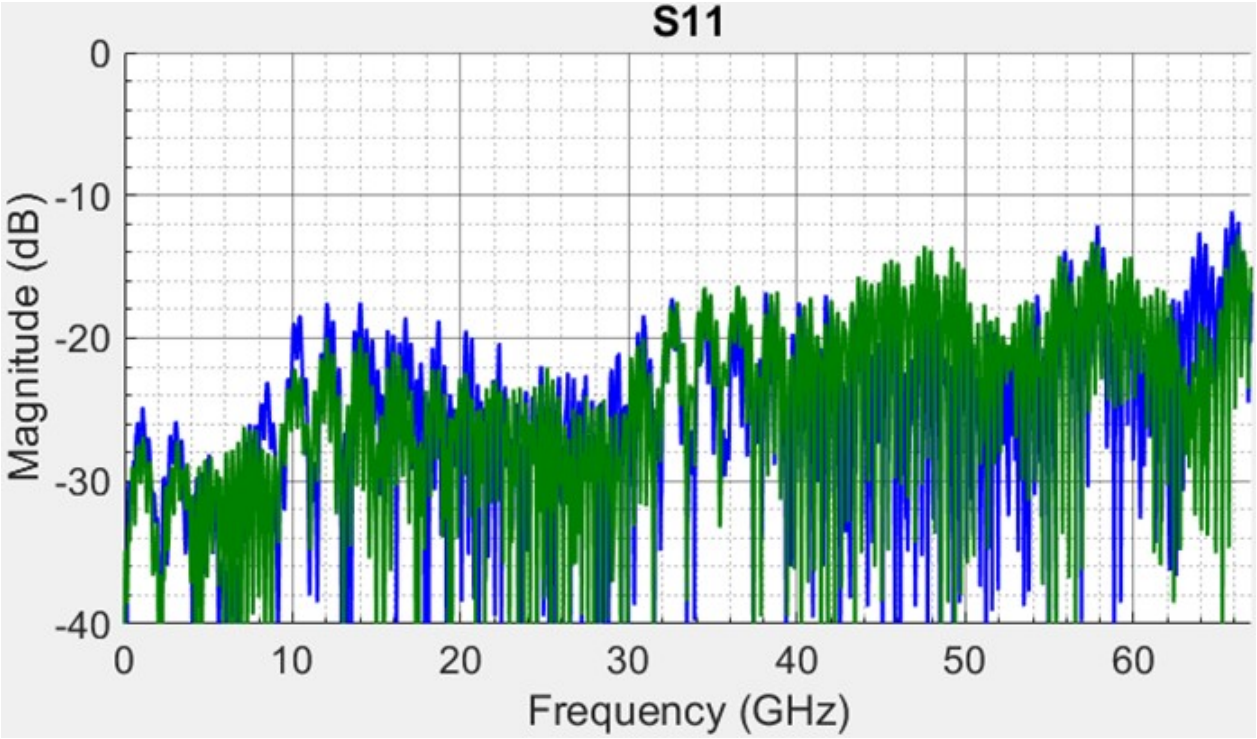
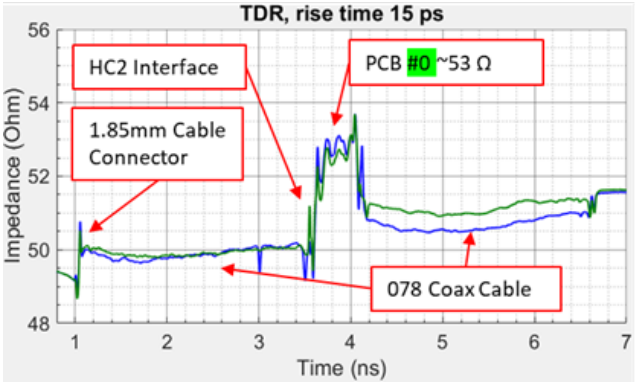
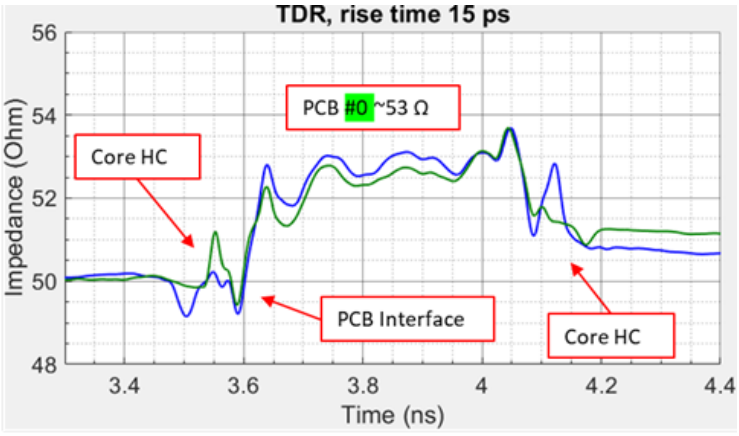
SIGNAL INTEGRITY REPORT

Return Loss (S11), Single-Ended

(CoreHC Channels: 3→4 & 11 → 2, Board Locations: J35, J36)







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1	EC No: N/A DATE: 04/ 12 / 2021	Core HC 2.5mm SIW: Configuration 1X2P (HC2 to PCB) CARLISLE IT CONFIDENTIAL	9 of 21

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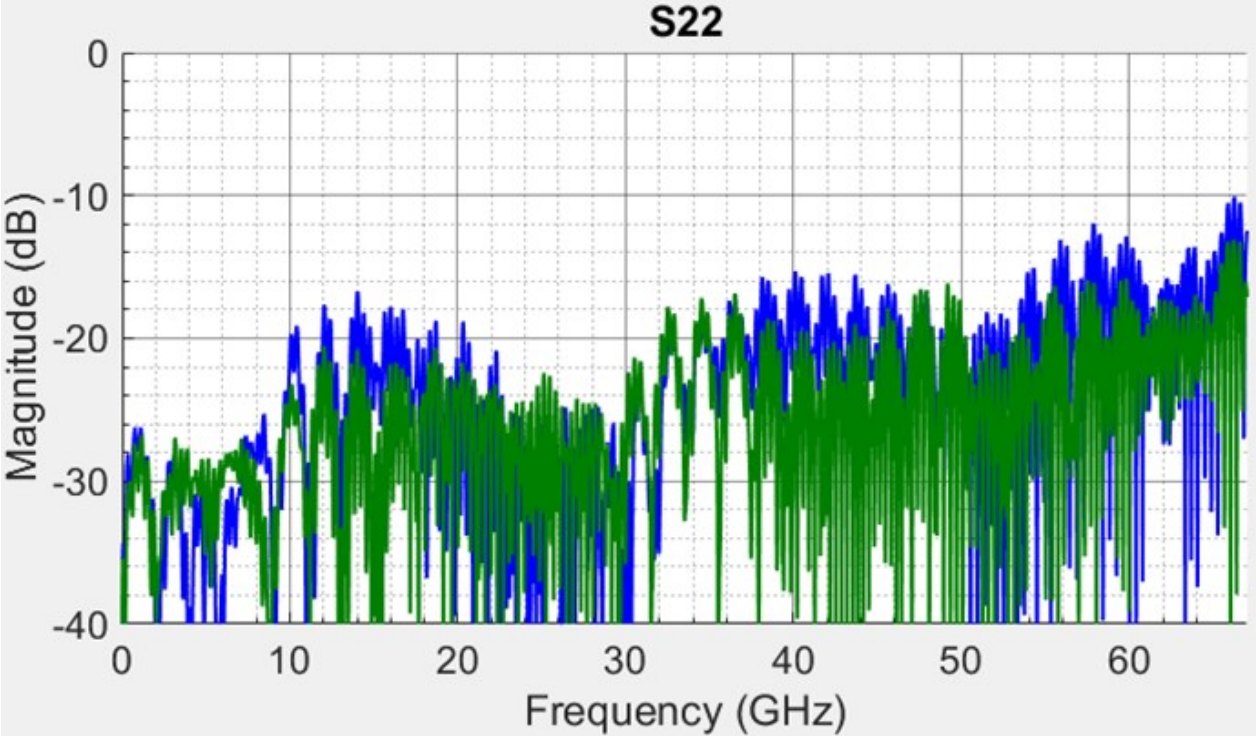
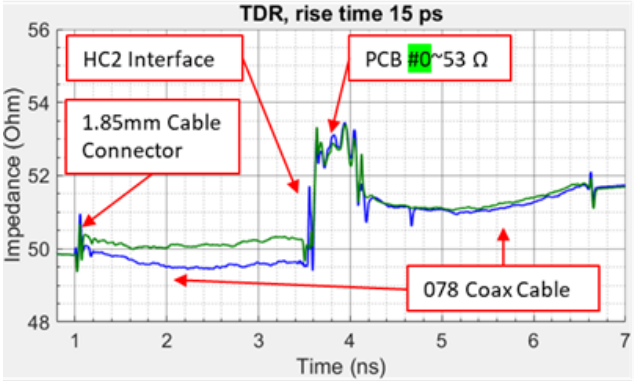
RSI-TM7SSSH22S8MS028	R.Stavoli	H.Tran	E.Soubh

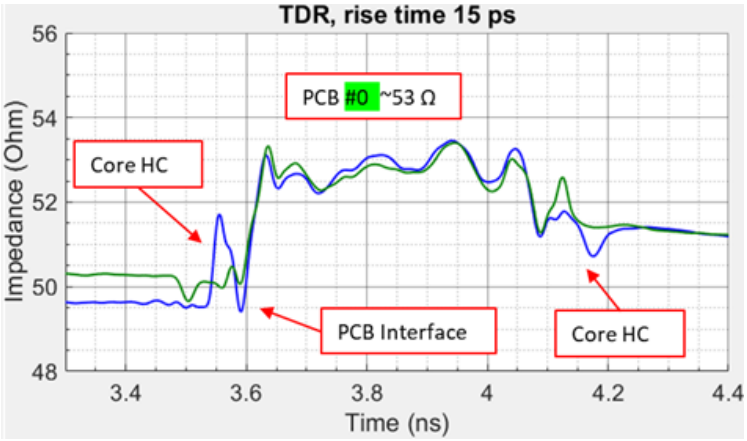
SIGNAL INTEGRITY REPORT

Return Loss (S22), Single-Ended

(CoreHC Channels: 3→4 & 11 → 2, Board Locations: J35, J36)







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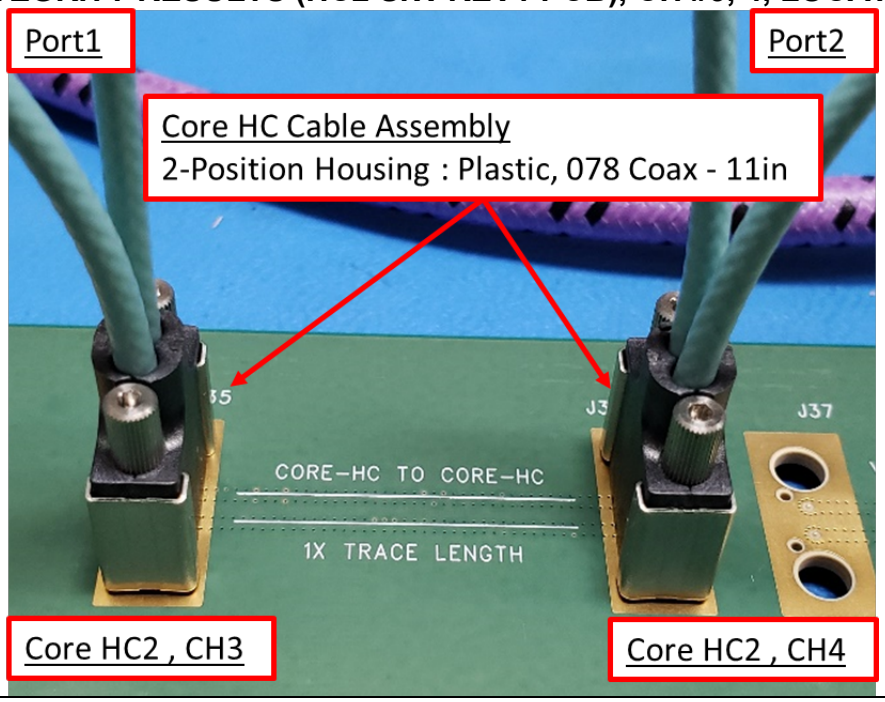
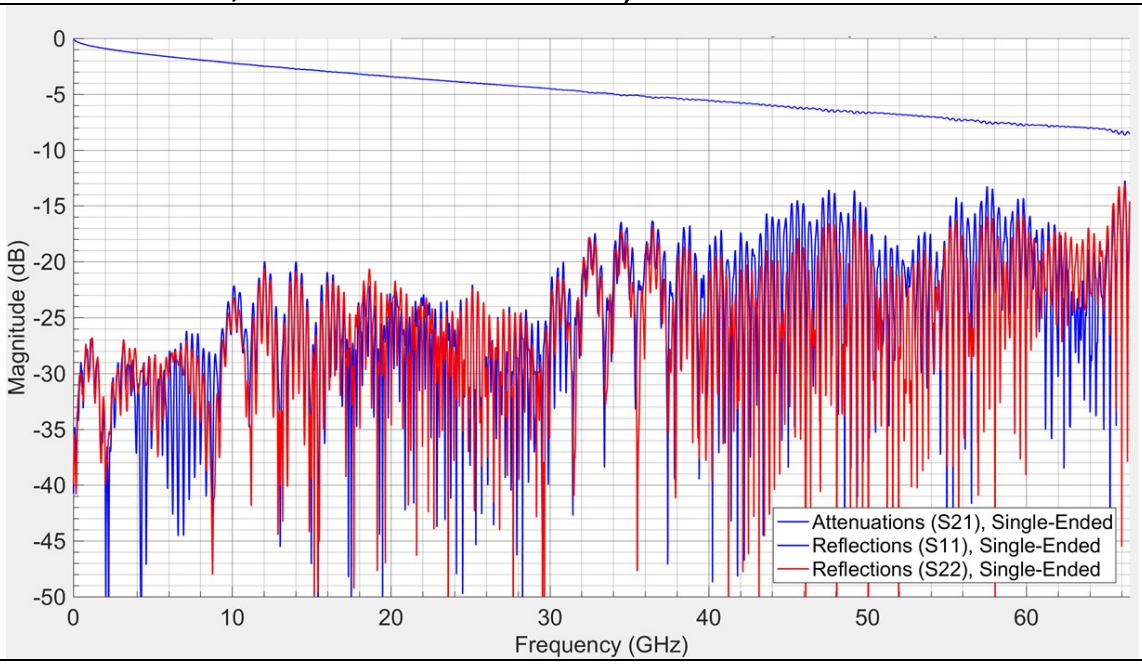
SIGNAL INTEGRITY REPORT

6.0 SIGNAL INTEGRITY RESULTS (HC2 SIW REV1 PCB), CH #3, 4, LOCATION J35-36



Insertion(S21) and Return (S11, S22) Loss, Single-Ended

(CoreHC Channel: 3 →4, Board Location: J35 → J36)



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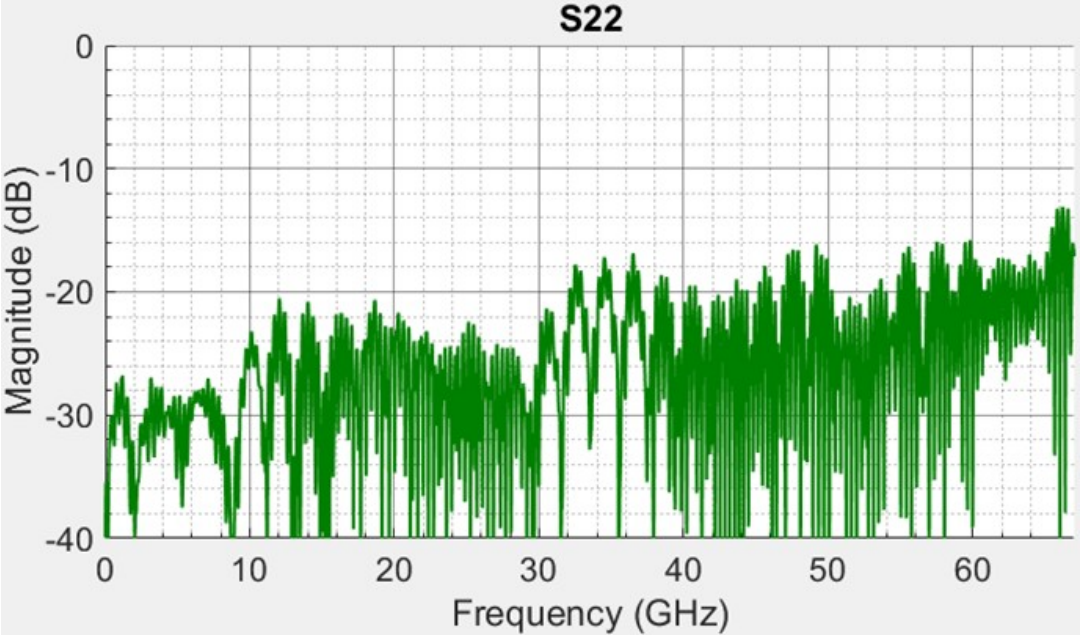
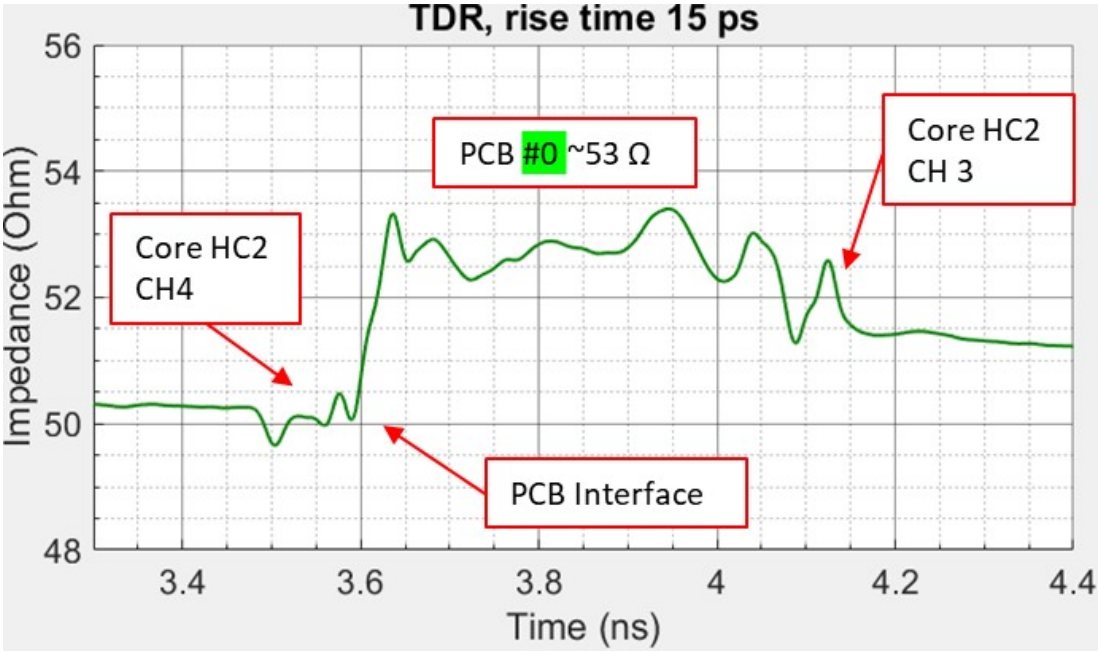
SIGNAL INTEGRITY REPORT

Return Loss (S22), Single-Ended

(CoreHC Channel: 3 →4, Board Location: J35 → J36)





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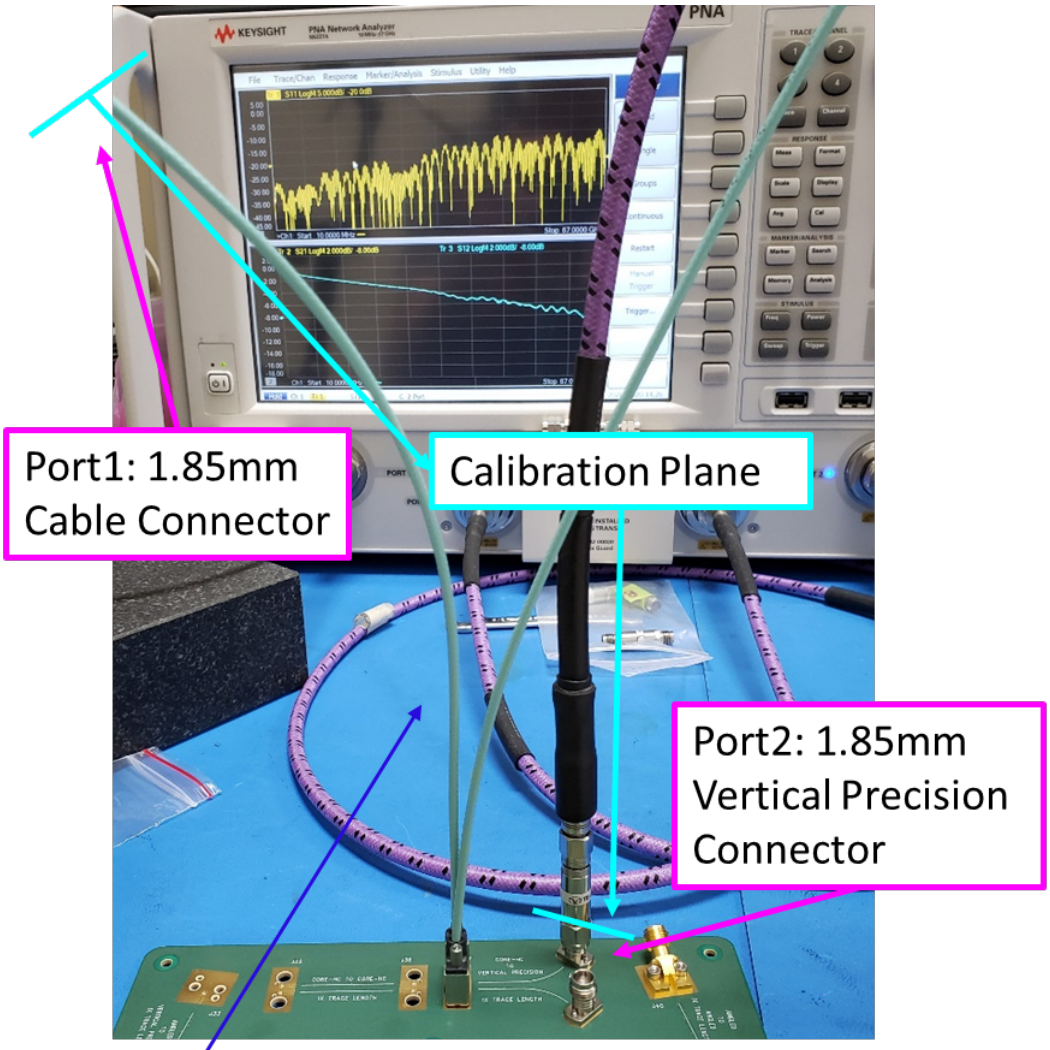
SIGNAL INTEGRITY REPORT

7.0 MEASUREMENT SET-UP, DE-EMBEDDING: CORE HC → 1.85 VERTICAL PREC. CONNECTOR

Port 1: Core HC (1.85mm Cable Connector) → Device Under Test → Port 2: 1.85mm Vertical Mount Precision Connector (TMB-V8F2-3L1)



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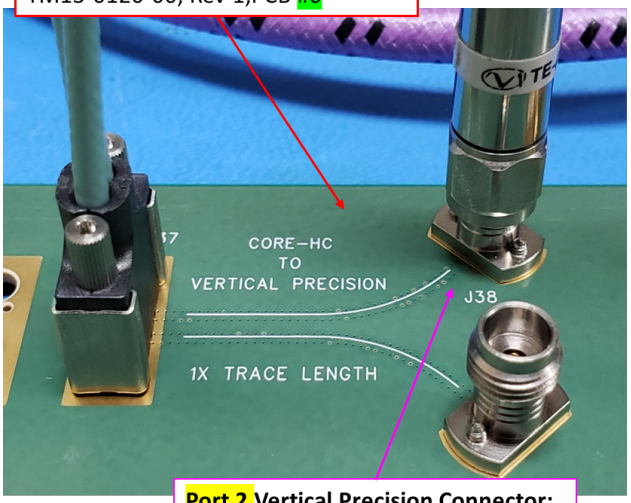
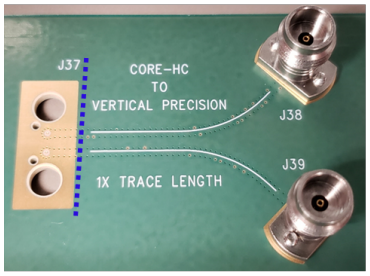
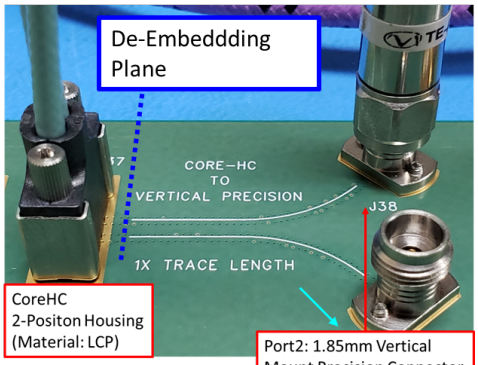
SIGNAL INTEGRITY REPORT

Core HC 32-Position Ring Eval Board
TM13-0120-00, Rev 1,PCB #0



Port 2 Vertical Precision Connector:
1.85mm, Vertical Mount
P/N: TMB-V8F2-3L1

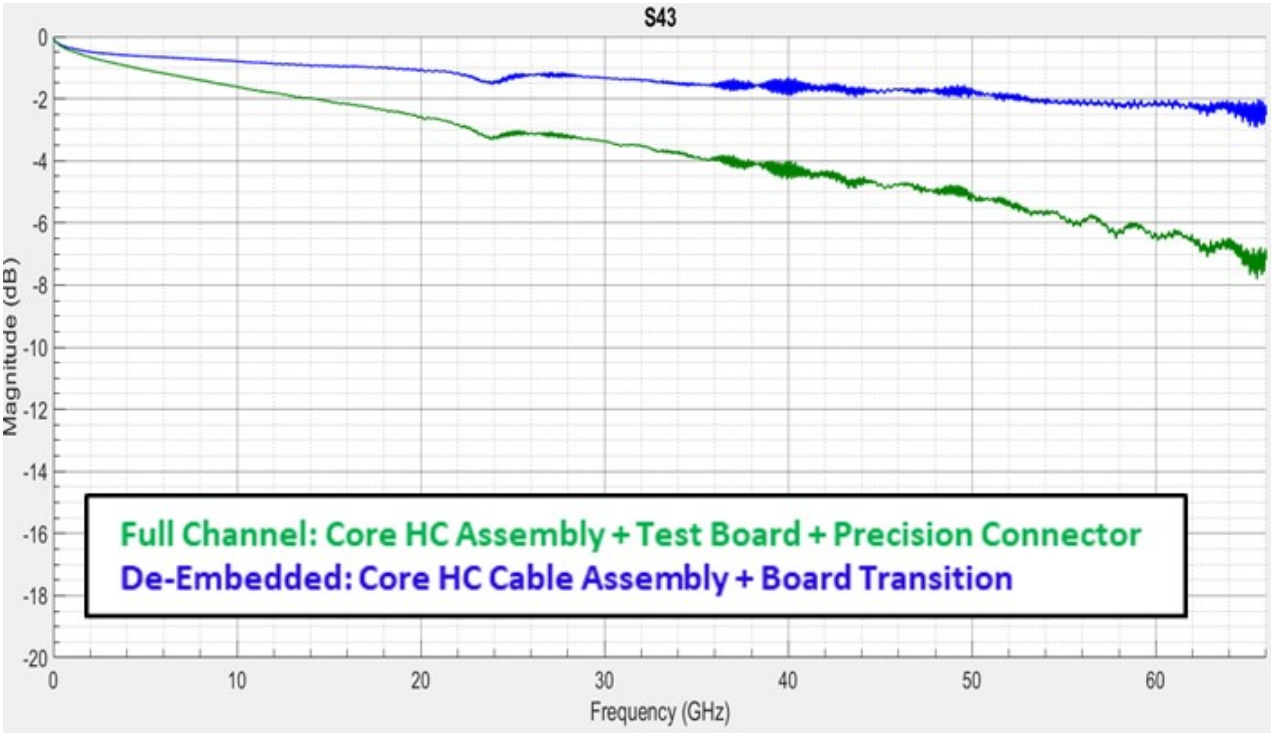




CoreHC
2-Positon Housing
(Material: LCP)

Port2: 1.85mm Vertical
Mount Precision Connector

Insertion Loss (S21), Single-Ended
(CoreHC Channels: 3, Board Locations: J39)



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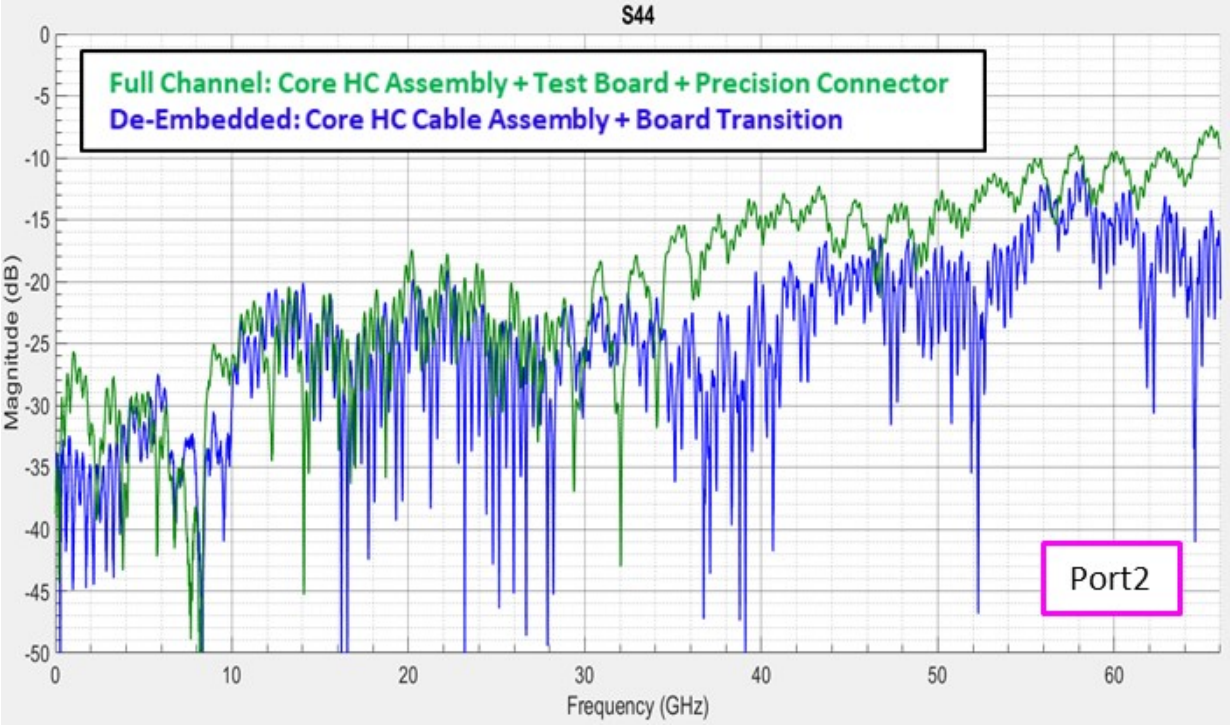
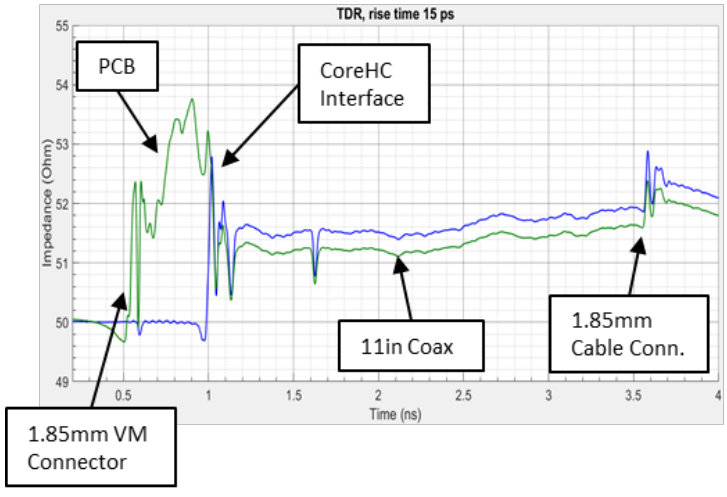
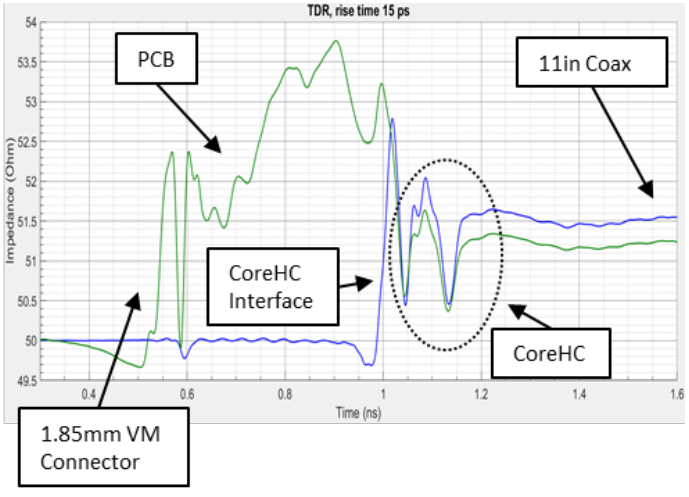
SIGNAL INTEGRITY REPORT

Return Loss (S22), Single-Ended

(CoreHC Channels: 3, Board Locations: J39)







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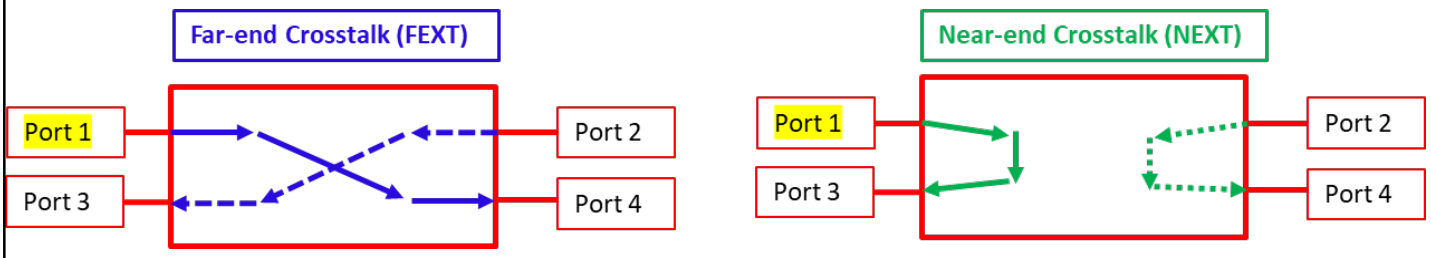
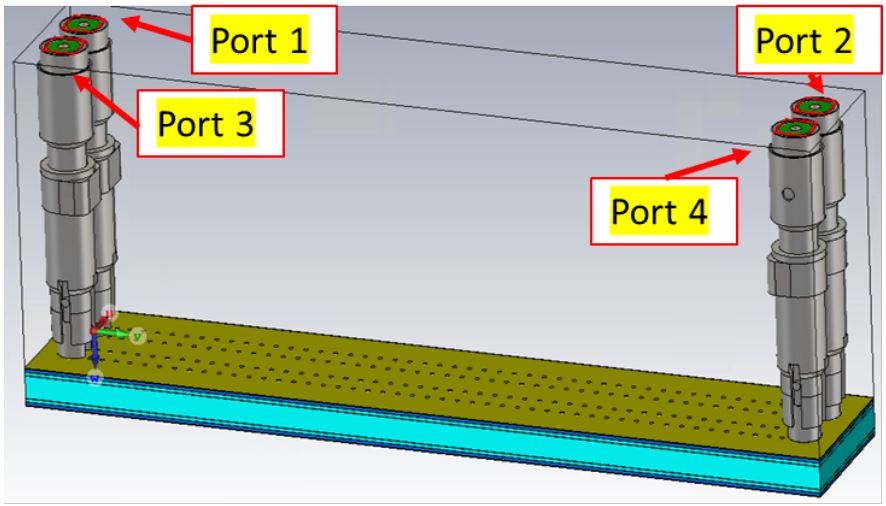
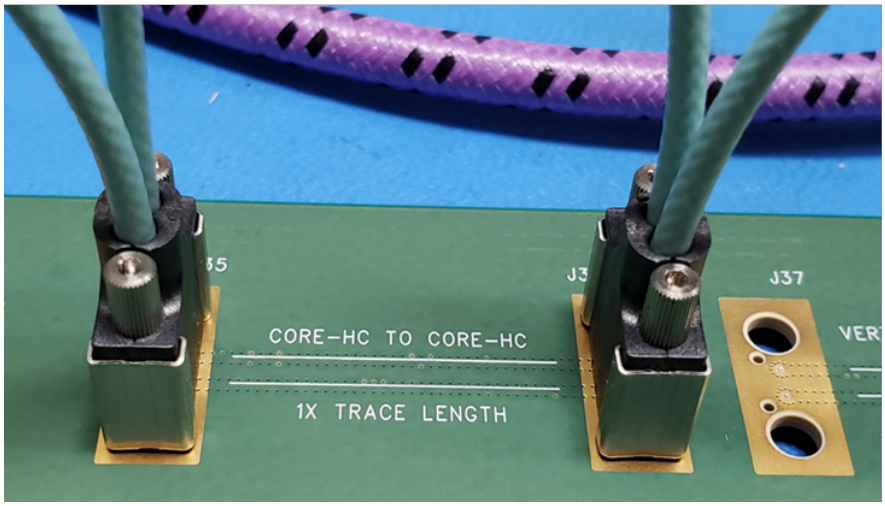
RSI-TM7SSSH22S8MS028	R.Stavoli	H.Tran	E.Soubh

8.0 MEASUREMENT SET-UP, SINGLE-ENDED, CROSSTALK (HC2 SIW REV1)





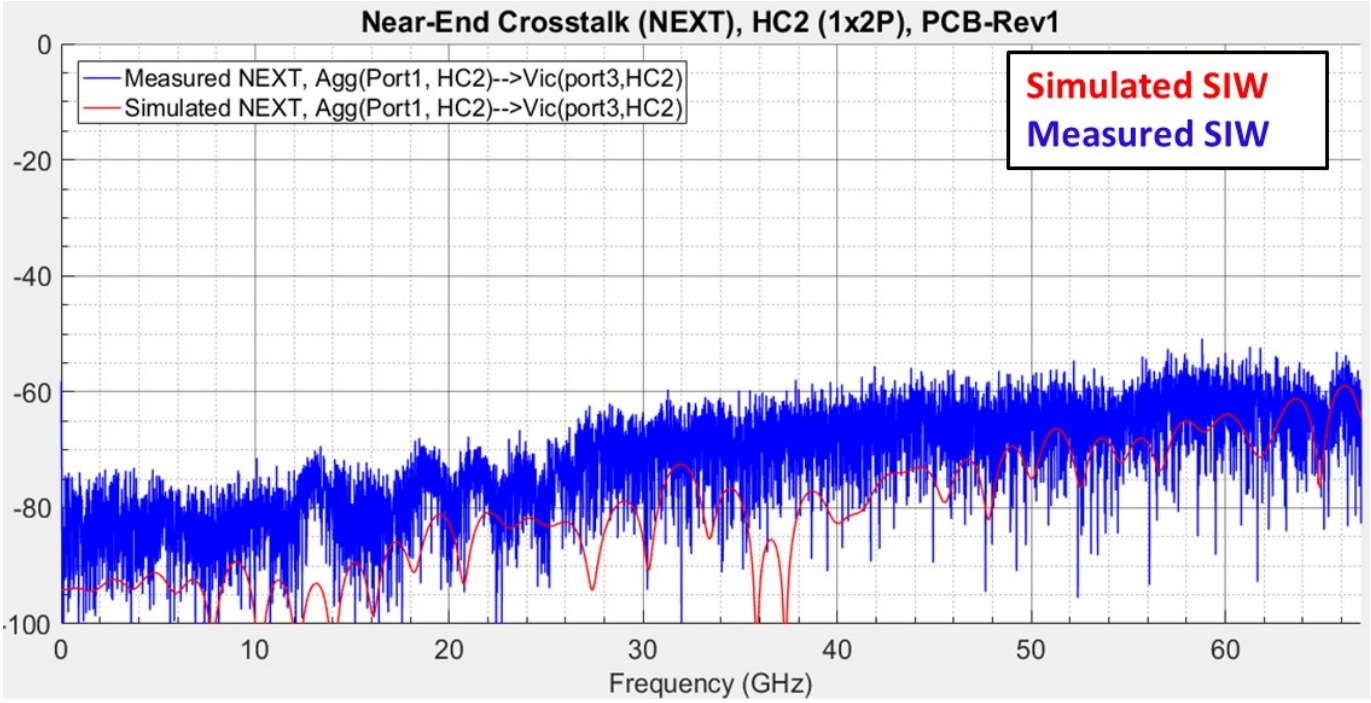


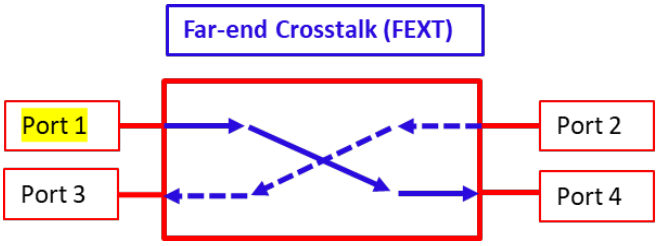
SIGNAL INTEGRITY REPORT

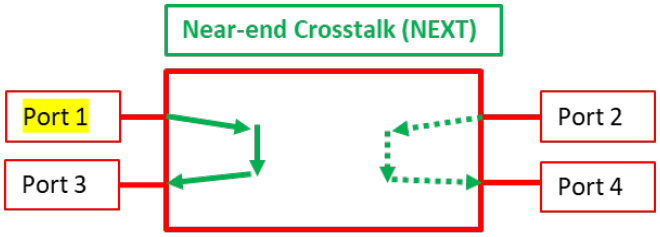
9.0 SIGNAL INTEGRITY RESULTS, SINGLE-ENDED, CROSSTALK (HC2 SIW REV1)

Near-End Crosstalk (S31), Single-Ended

(CoreHC Channels: 3, 11, Board Locations: J35), Port1(HC2-CH11) → Port3(HC2-CH3)







REVISION:	ECN INFORMATION:	TITLE:	SHEET No.
1	EC No: N/A DATE: 04/ 12 / 2021	Core HC 2.5mm SIW: Configuration 1X2P (HC2 to PCB) CARLISLE IT CONFIDENTIAL	17 of 21

DOCUMENT NUMBER:	SI ENGINEER:	DESIGN ENGINEER	ENGINEERING MANAGER
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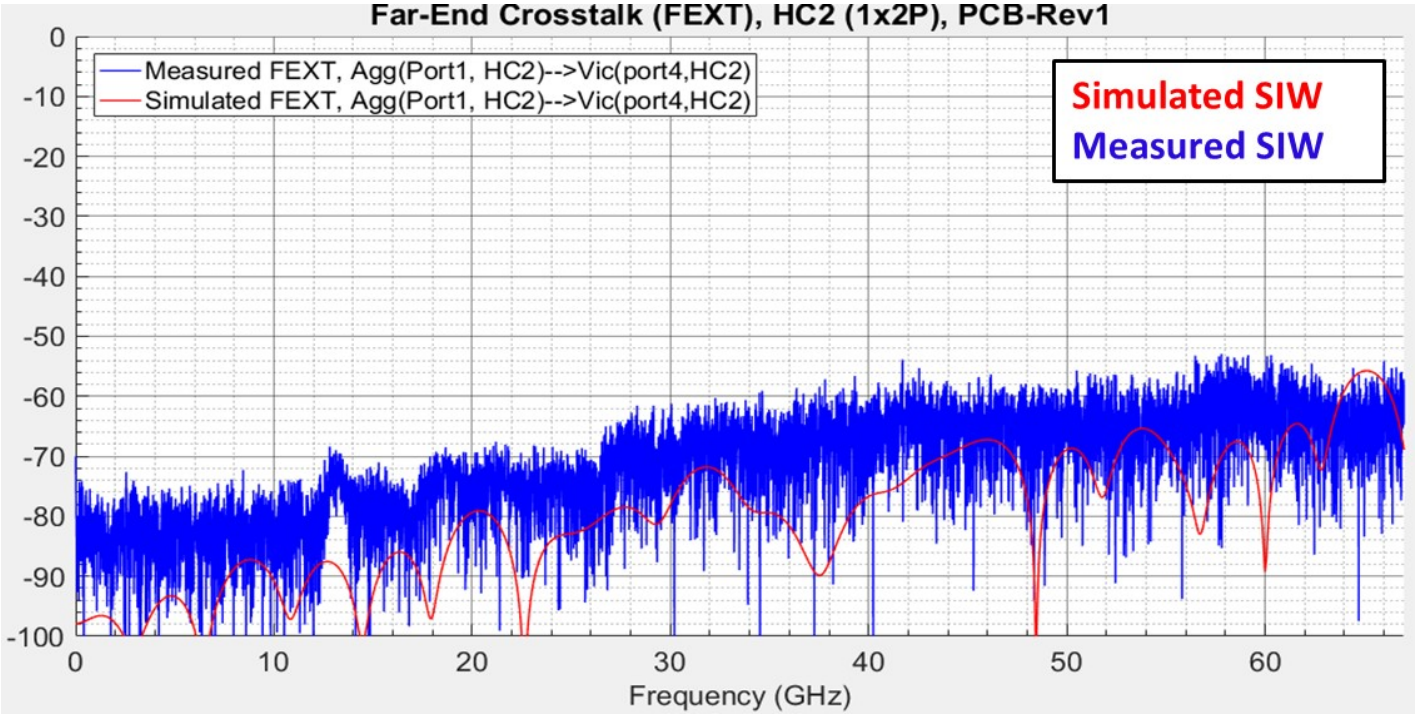
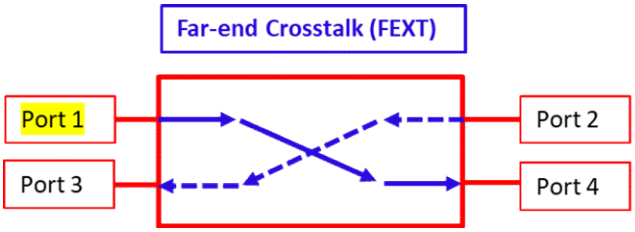
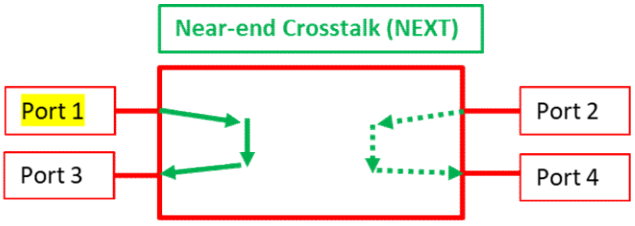
SIGNAL INTEGRITY REPORT

Far-End Crosstalk (S41), Single-Ended

(CoreHC Channels:11, Board Locations: J35/J36), Port1(HC2-CH11) → Port 4 (VMSIW/PCB)





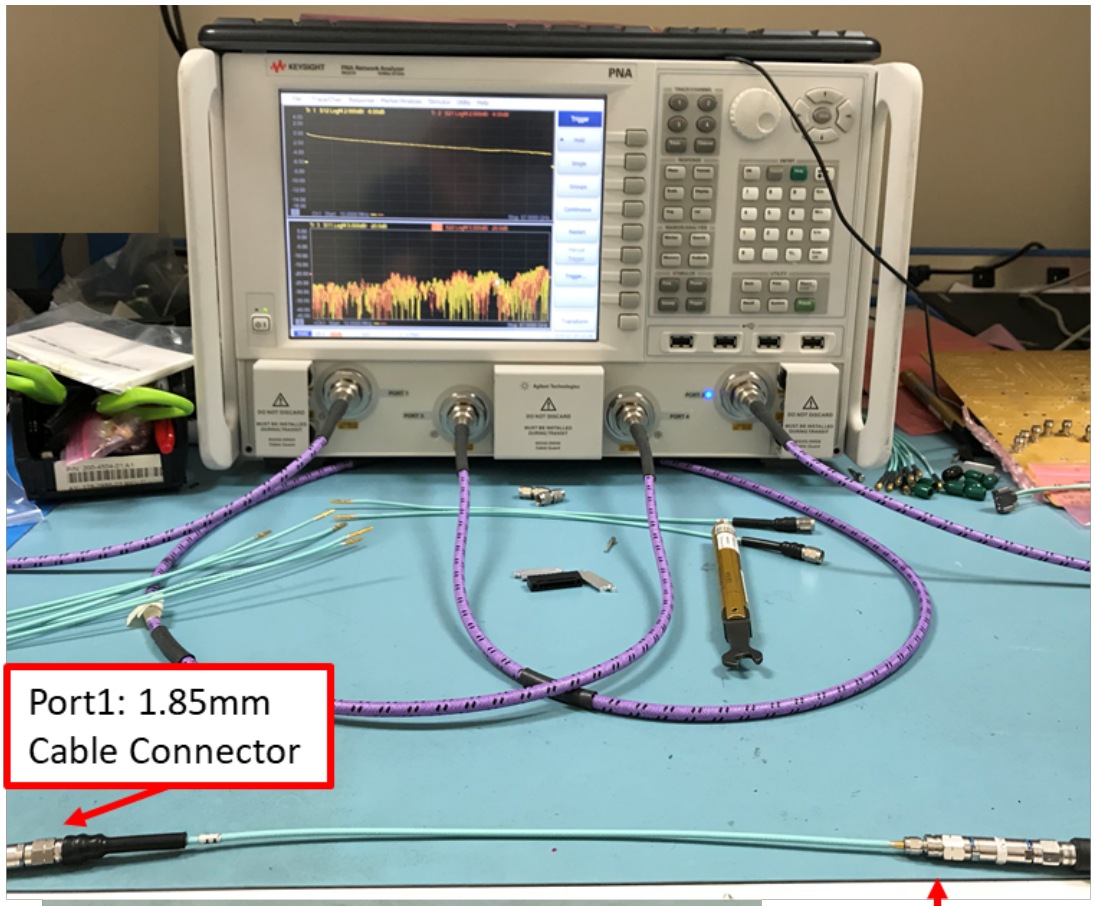


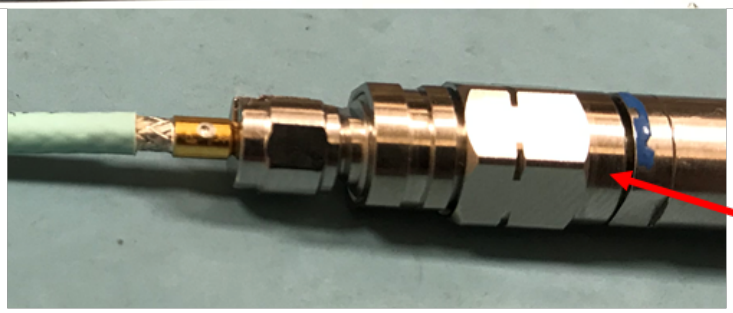
REVISION:	ECN INFORMATION:	TITLE:	SHEET No.
1	EC No: N/A DATE: 04/ 12 / 2021	Core HC 2.5mm SIW: Configuration 1X2P (HC2 to PCB) CARLISLE IT CONFIDENTIAL	18 of 21

DOCUMENT NUMBER:	SI ENGINEER:	DESIGN ENGINEER	ENGINEERING MANAGER
RSI-TM7SSSH22S8MS028	R.Stavoli	H.Tran	E.Soubh

10.0 MEASUREMENT SET-UP (HC2 1.85MM RF ADAPTOR #1)

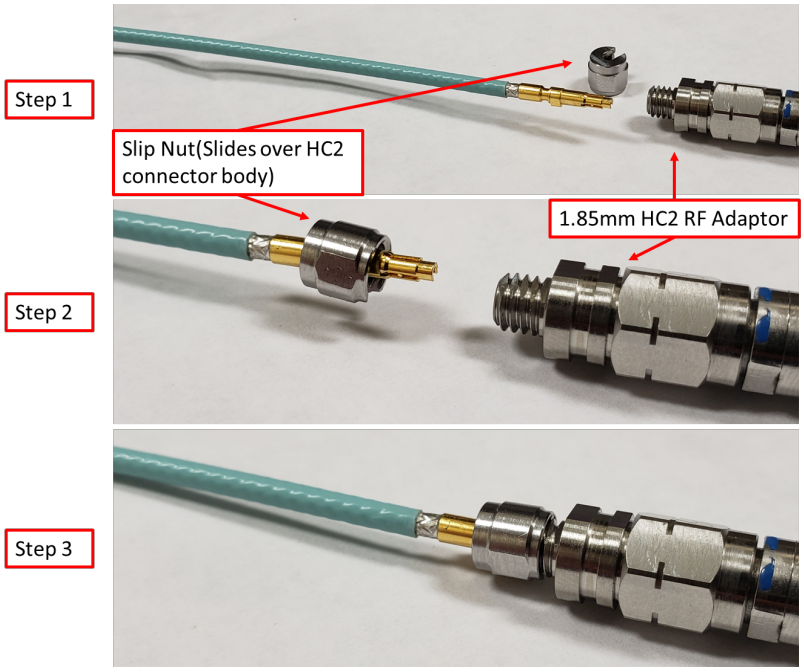
Port 1: Core HC (1.85mm Cable Connector) → Device Under Test → Port 2: Core HC Interface (1.85mm RF Core HC Adaptor #1)





SIGNAL INTEGRITY REPORT

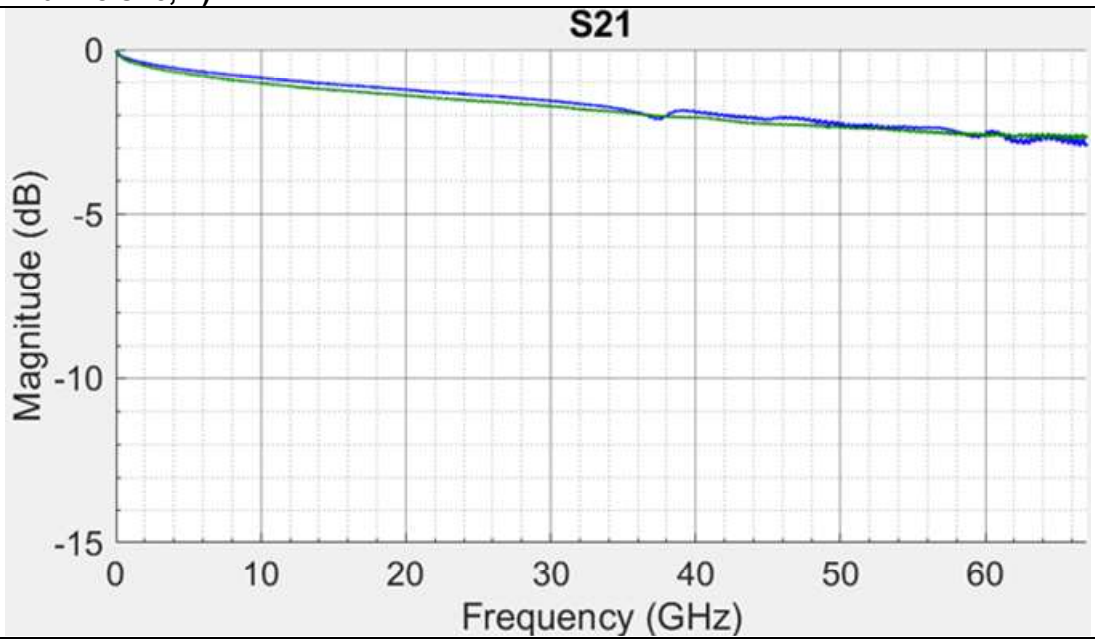
HC2 Adaptor Testing Procedure



11.0 SIGNAL INTEGRITY RESULTS (HC2 1.85MM RF ADAPTOR #1)

Insertion Loss (S21), Single-Ended

(CoreHC Channels: 3, 4)



REVISION:	ECN INFORMATION:	TITLE:	SHEET No.
1	EC No: N/A DATE: 04/ 12 / 2021	Core HC 2.5mm SIW: Configuration 1X2P (HC2 to PCB) CARLISLE IT CONFIDENTIAL	20 of 21

DOCUMENT NUMBER:	SI ENGINEER:	DESIGN ENGINEER	ENGINEERING MANAGER
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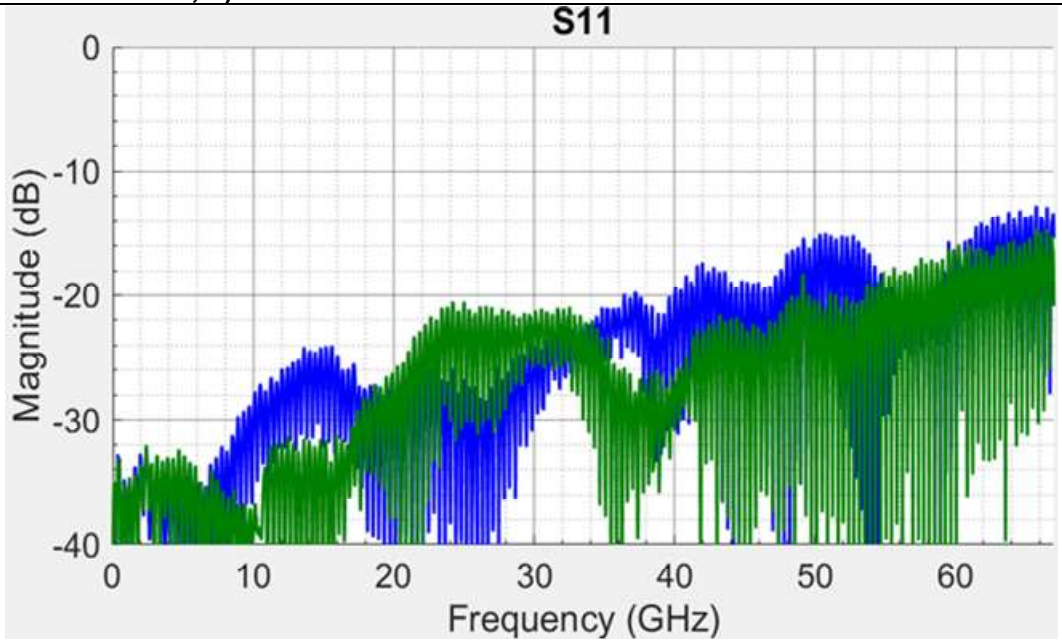
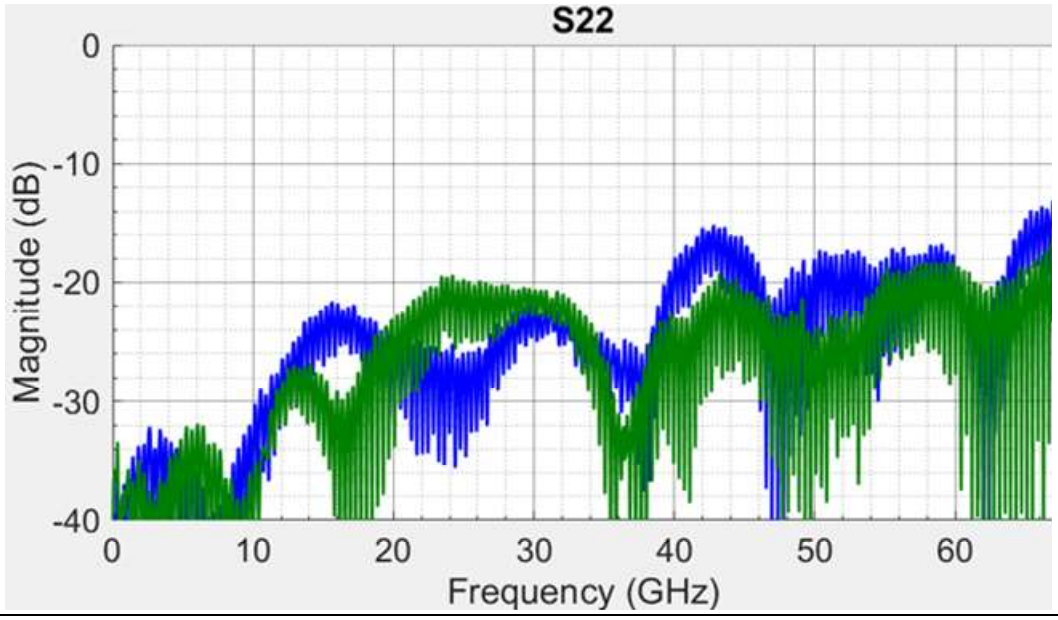
Return Loss (S11, S22), Single-Ended

(CoreHC Channels: 3, 4)





12.0 APPENDIX, (SPARAMETERS SHOWN IN REPORT)

CoreHC Reference Cable Assembly_SIW_2-Position Measurements_041221 4/12/2021 7:54 PM Compressed (zipp... 5,145 KB