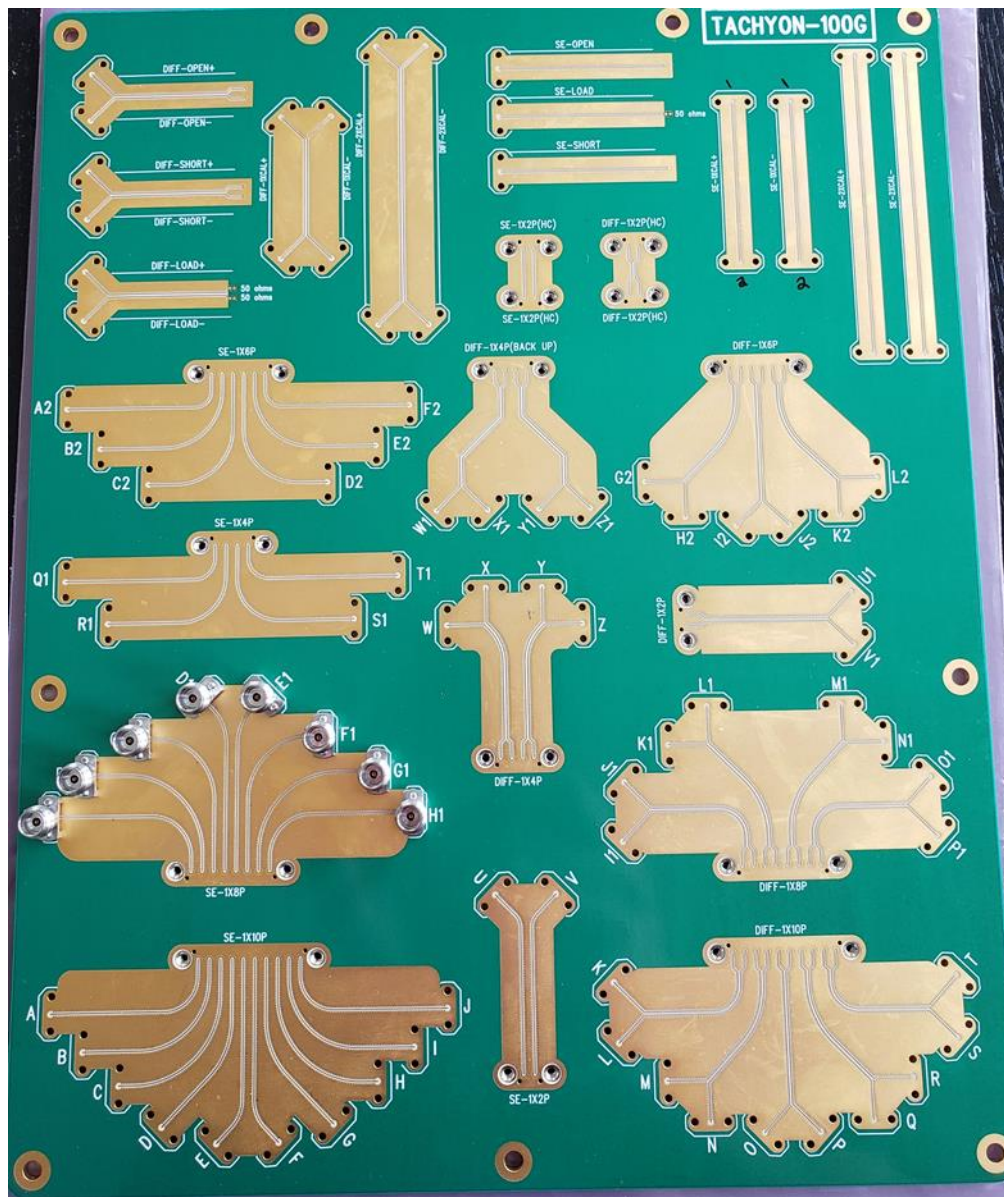


# SIGNAL INTEGRITY REPORT

## Test and Measurement Performance Report

Part Number TM7SSSH22S8MS028 (Core HC)

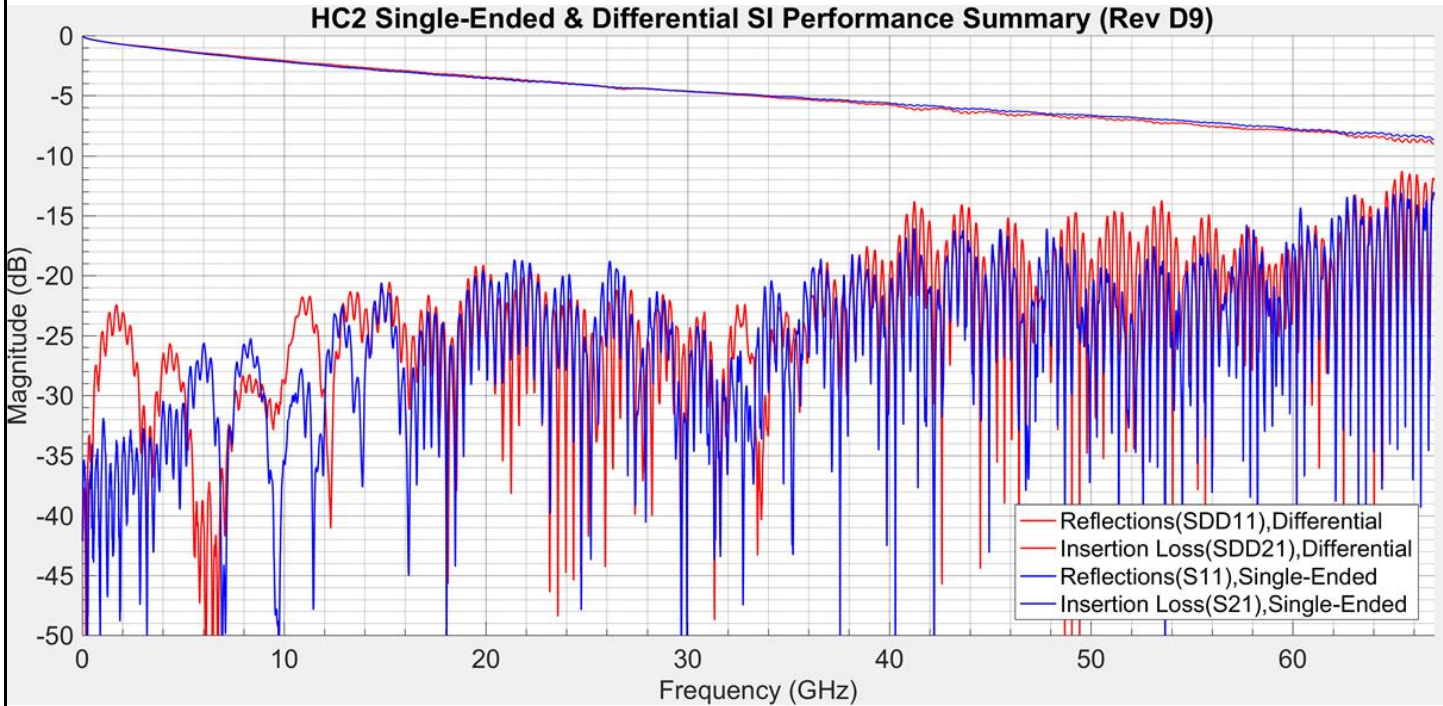
Distribution: Internal and External Use



<u>REVISION:</u>  <b>1</b>	<u>ECN INFORMATION:</u> EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	<u>TITLE:</u> <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> <b>CARLISLE IT CONFIDENTIAL</b>	<u>SHEET No.</u>  <b>1 of 22</b>
<u>DOCUMENT NUMBER:</u> <b>RSI-TM7SSSH22S8MS028</b>	<u>SI ENGINEER:</u> <b>R.Stavoli</b>	<u>DESIGN ENGINEER</u> <b>H.Tran</b>	<u>ENGINEERING MANAGER</u> <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			

# SIGNAL INTEGRITY REPORT

## SI Performance Summary (Attenuation & Reflections, Single-Ended, Differential)



**Legend:** Single-Ended, Differential

\* For further details regarding the testing setup and configuration please see the rest of the report.

<b>REVISION:</b> <b>1</b>	<b>ECN INFORMATION:</b> EC No: <b>N/A</b> DATE: <b>05/ 26 / 2020</b>	<b>TITLE:</b> <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> <b>CARLISLE IT CONFIDENTIAL</b>	<b>SHEET No.</b> <b>2 of 22</b>
<b>DOCUMENT NUMBER:</b> <b>RSI-TM7SSSH22S8MS028</b>	<b>SI ENGINEER:</b> <b>R.Stavoli</b>	<b>DESIGN ENGINEER</b> <b>H.Tran</b>	<b>ENGINEERING MANAGER</b> <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			



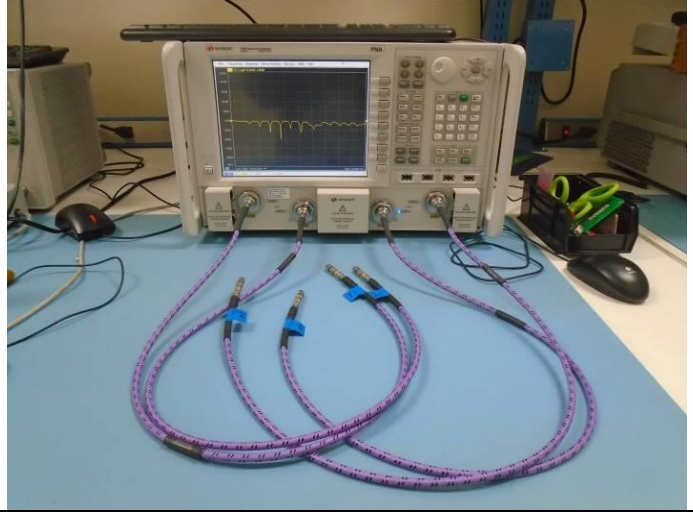
# SIGNAL INTEGRITY REPORT

## 1.0 TEST SETUP AND DUT

### Equipment, fixtures, and methods

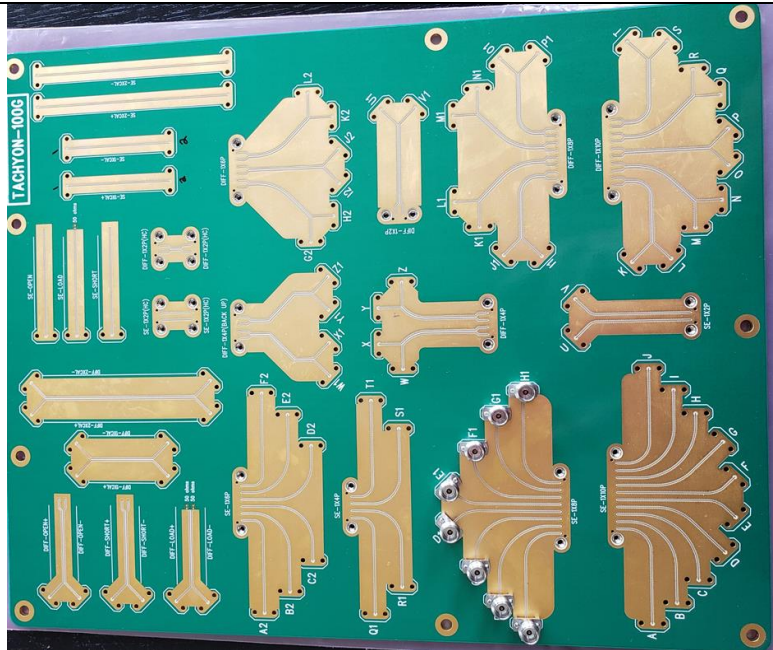
**Test method:** All data measured from test PCB shown below and a N5227A PNA Network Analyzer

- Calibration was performed up to the 1.85mm SMA adapters using calibration kit: 85058B
- Data was swept from 10 MHz to 67GHz for 6700 points
- Data averaging was turned off.
- Data is not dembedded and includes the board traces and the Core HC cable assembly



### Assembly Description

- T&M PN: TM7SSSH22S8MS028
- 2- Position LCP Connector Housing, two pieces at the interface
- **11-inch solid center conductor 092 coax cable**
- Carlisle DUT PCB: Core HC, CPW, Vertical Launch, **Rev D, #9**
- Port 1: 1.85mm Cable Connector (Core HC)
- Port 2: 1.85mm CPW Vertical Launch Precision Connector (on HC2, CPW PCB)



### Testing Samples:

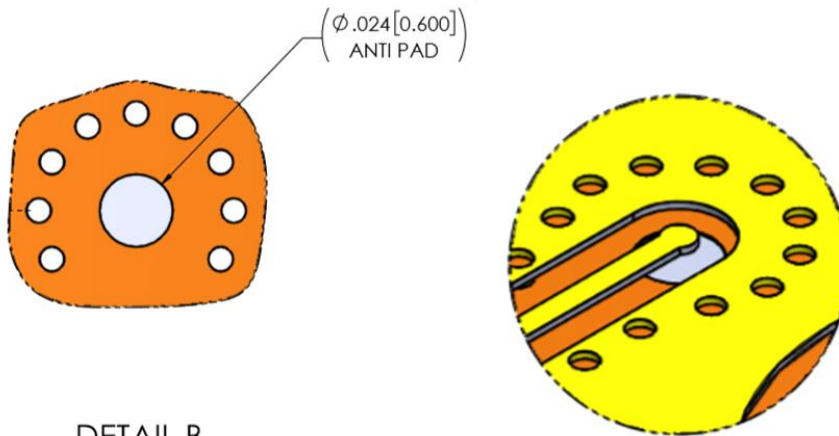
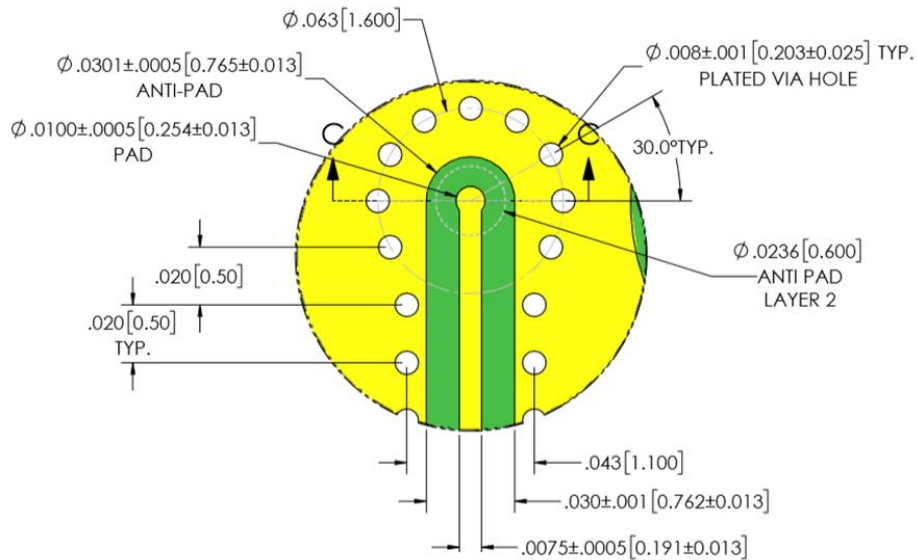
- 1 Samples
- 2 Channels
- 2 THRU Measurements w/ PCB (2 Channels x 1 samples) -> **Single-Ended**
- 4 Crosstalk Meas. w/PCB (FEXT, NEXT) -> **Single-Ended**
- 1 THRU Meas. w/ PCB (1 Channels x 1 samples) -> **Differential**
- 2 THRU Meas. w/RF Adaptor (2 Chan. x 1 samples) -> **Single-Ended**

REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> <b>CARLISLE IT CONFIDENTIAL</b>	SHEET No. <b>3 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC			

# SIGNAL INTEGRITY REPORT

## 2.0 BOARD STACKUP & FOOTPRINT INFORMATION

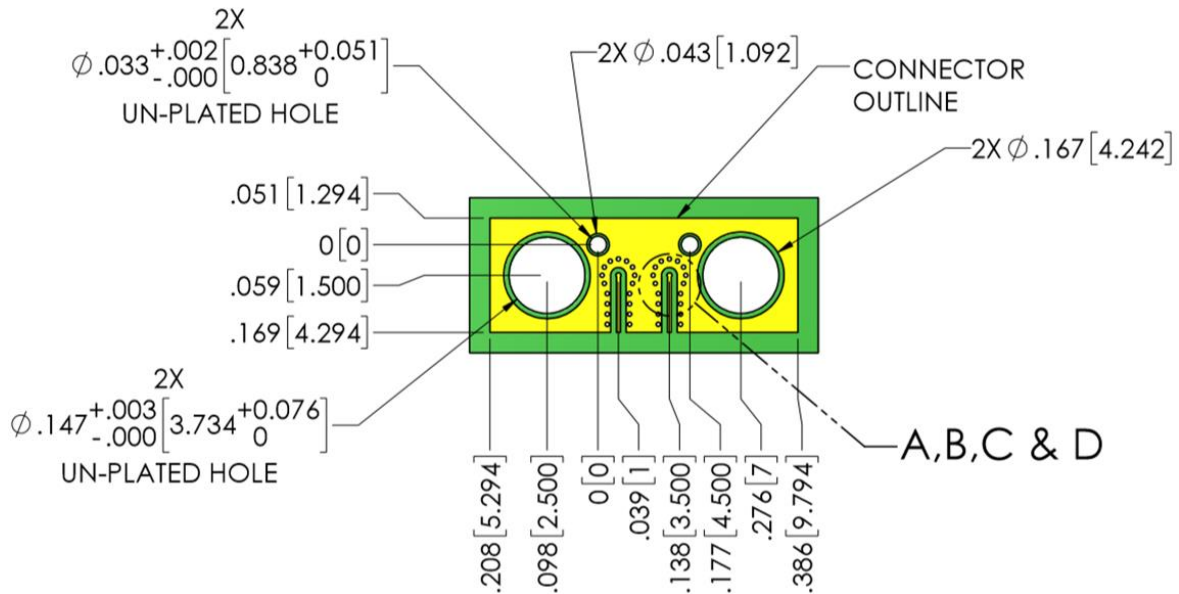
- Carlisle Core HC 2.5mm CPW Test Board
  - Revision D, #9, Coplanar Waveguide, Vertical Launch
  - **Cable Assembly placed on 2-Position Single-Ended Footprint**
- Dielectric Material: Tachyon 100G (Dk.2.97, Df 0.0014 @ 20 GHz)
  - Thickness: 0.104mm / 4.11 mil
  -



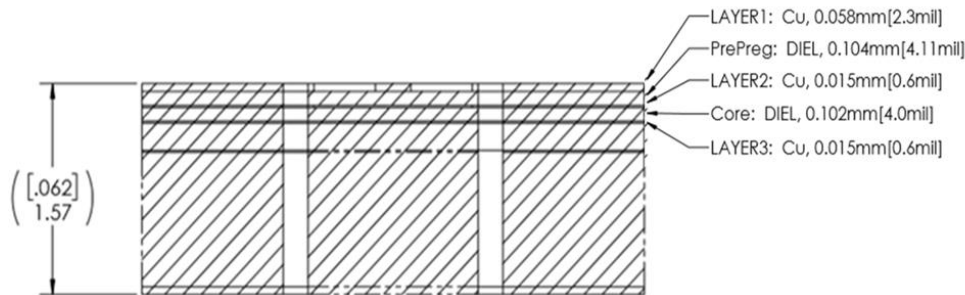
DETAIL B  
SCALE 32 : 1  
LAYER2

REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>4 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC			

# SIGNAL INTEGRITY REPORT



## Core HC 2.5mm CPW Test Board Stackup (RevD0)



### C) PCB FINISH

#### 1. Surface Protective Plating

- All exposed copper on the outer layers shall be plated with a protective surface finish.
- All exposed pads, edge fingers and plated through holes shall be ENIG with thickness listed in Table 2.

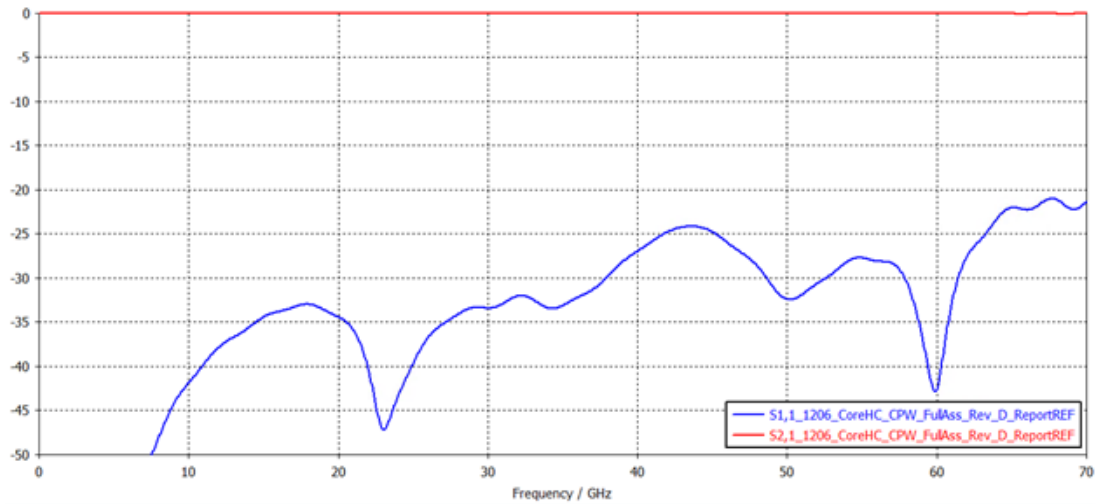
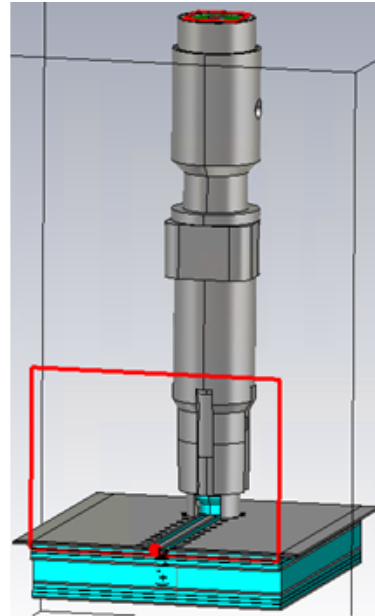
Table 2: Protective Plating Thickness

Nickel		Immersion Gold	
µm (microinch)		µm (microinch)	
Min.	Max.	Min.	Max.
2.5 (100)	13(512)	0.051 (2)	0.2032 (8)

REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/ 26 / 2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> <b>CARLISLE IT CONFIDENTIAL</b>	SHEET No. <b>5 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC			

# SIGNAL INTEGRITY REPORT

**Simulated Data (CST)  
1 connector to PCB**



CoreHC_RevD_CPW_1206_032619_FullAss_SE_Rev_1.s2p	3/26/2019 4:26 PM	S2P File	147 KB
CoreHC_2p5mm_PCB_RevD_03262019_CPW_SE_Rev_1.stp	3/26/2019 4:35 PM	STP File	1,042 KB
CoreHC_2p5mm_InterconnectOnly+SolderConnections_03112019_Rev_1	3/11/2019 12:01 PM	STP File	1,415 KB

<b>REVISION:</b>  <b>1</b>	<b>ECN INFORMATION:</b> EC No: <b>N/A</b> DATE: <b>05/ 26 / 2020</b>	<b>TITLE:</b> <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> <b>CARLISLE IT CONFIDENTIAL</b>	<b>SHEET No.</b>  <b>6 of 22</b>
<b>DOCUMENT NUMBER:</b> <b>RSI-TM7SSSH22S8MS028</b>	<b>SI ENGINEER:</b> <b>R.Stavoli</b>	<b>DESIGN ENGINEER</b> <b>H.Tran</b>	<b>ENGINEERING MANAGER</b> <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			



# SIGNAL INTEGRITY REPORT

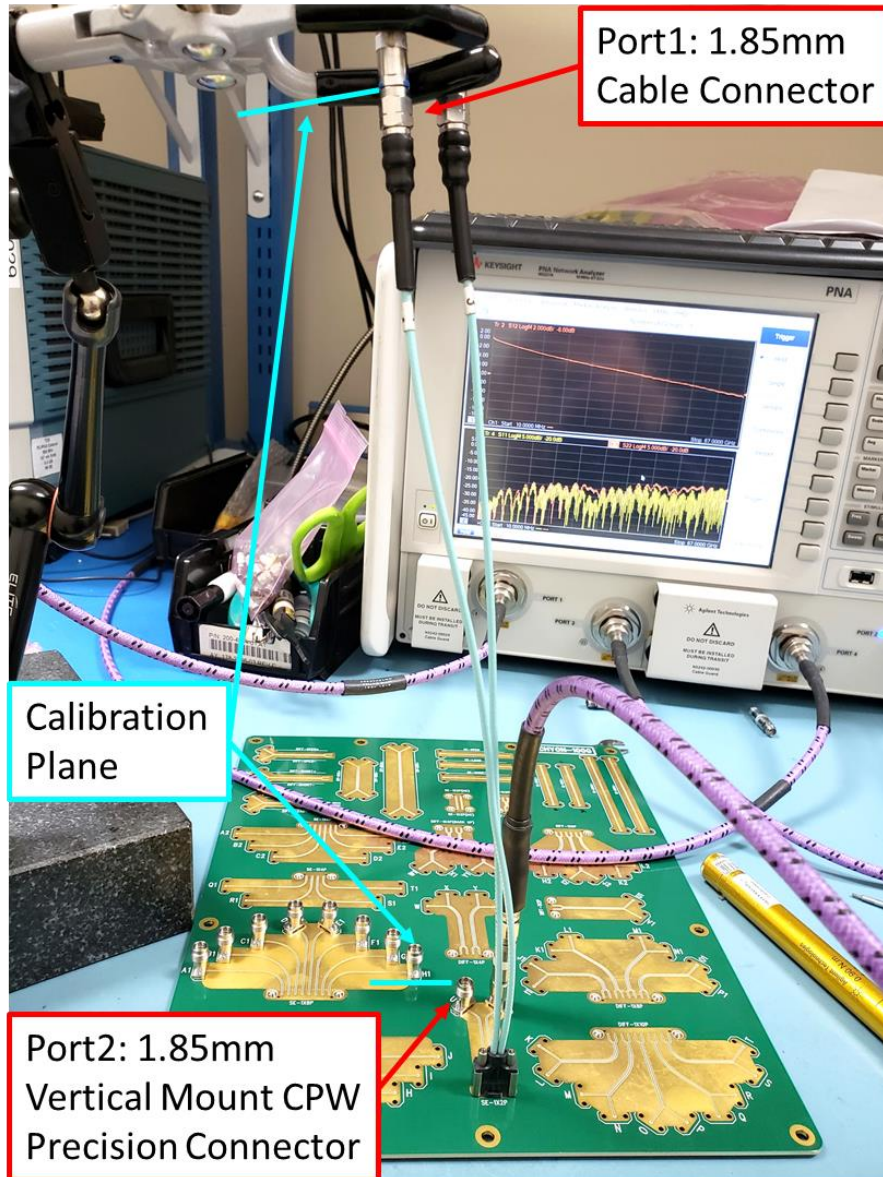
## 3.0 MEASUREMENT SET-UP, SINGLE-ENDED (HC2 CPW REVD BOARD)

Port 1: Core HC  
(1.85mm Cable Connector)

Device Under Test

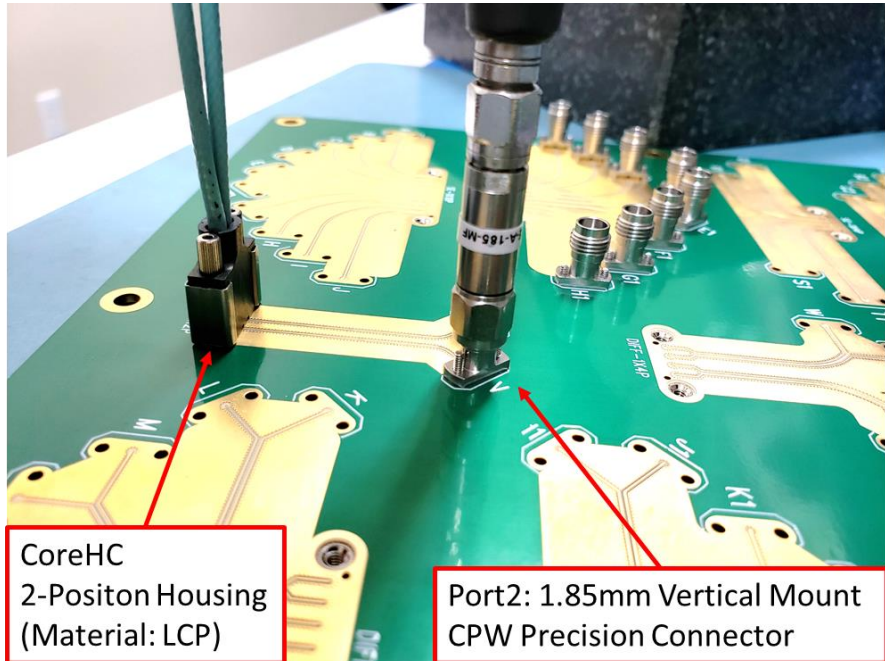
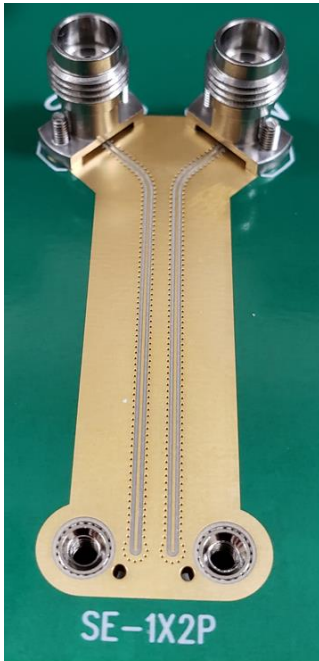
Port 2: Core HC RevD PCB  
(1.85mm CPW Vertical Mount  
Precision Connector)

Measurements are not dembedded and include the Core HC assembly (cable connector, cable, interconnect), PCB (transitions, traces) and 1.85mm CPW vertical mount precision connector.



REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/ 26 / 2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>7 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC			

# SIGNAL INTEGRITY REPORT

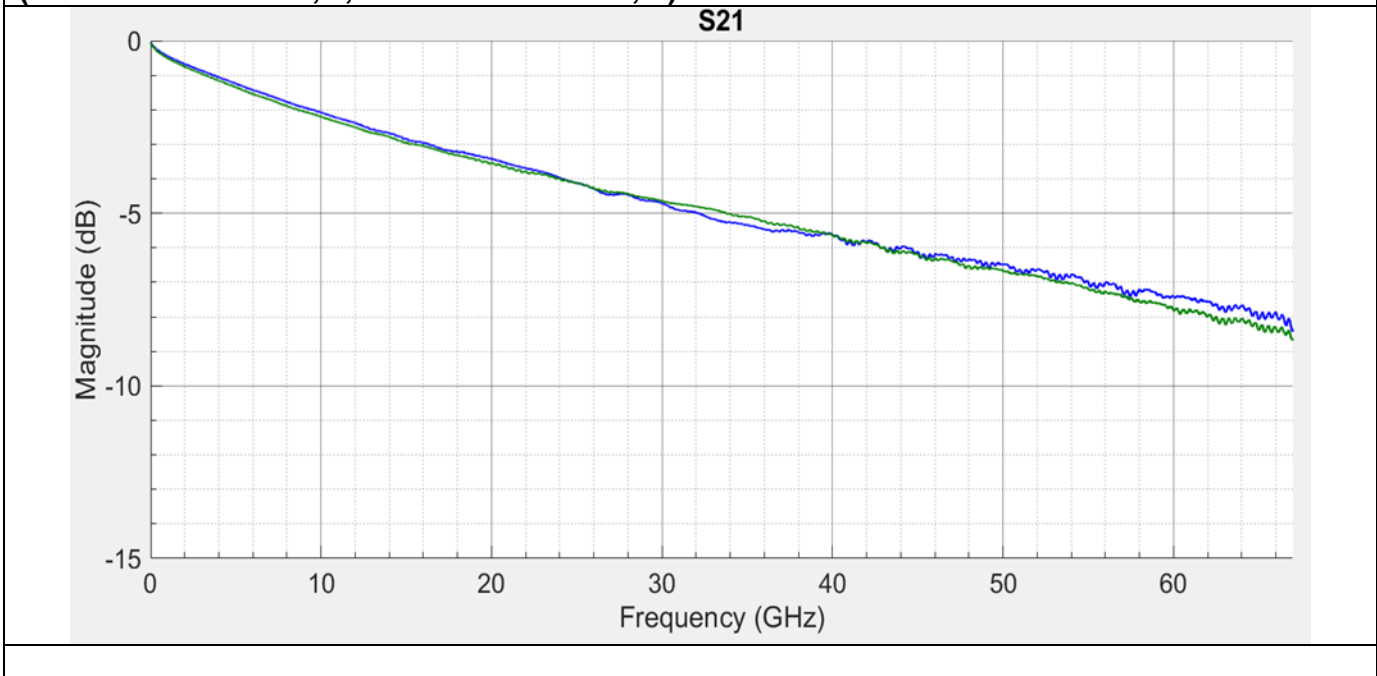


CoreHC  
2-Positon Housing  
(Material: LCP)

Port2: 1.85mm Vertical Mount  
CPW Precision Connector

## 4.0 SIGNAL INTEGRITY RESULTS, SINGLE-ENDED (HC2 CPW REVD BOARD)

### Insertion Loss (S21), Single-Ended (CoreHC Channels: 3, 4, Board Locations: U, V)

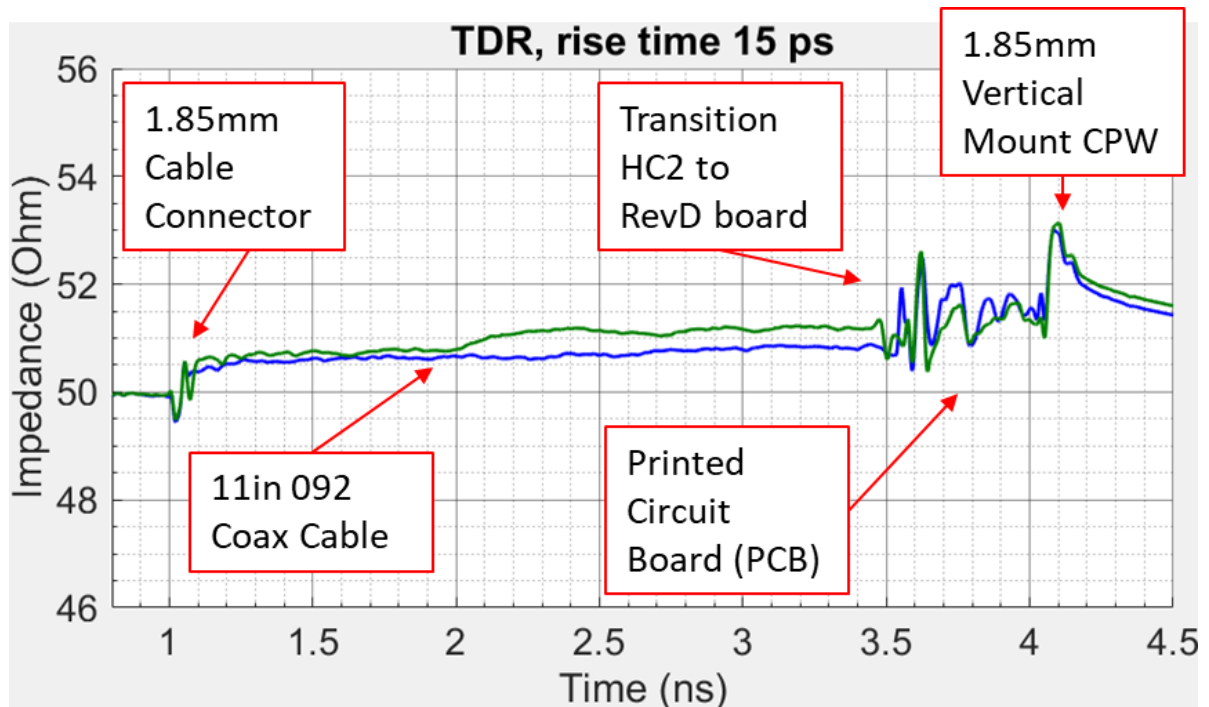
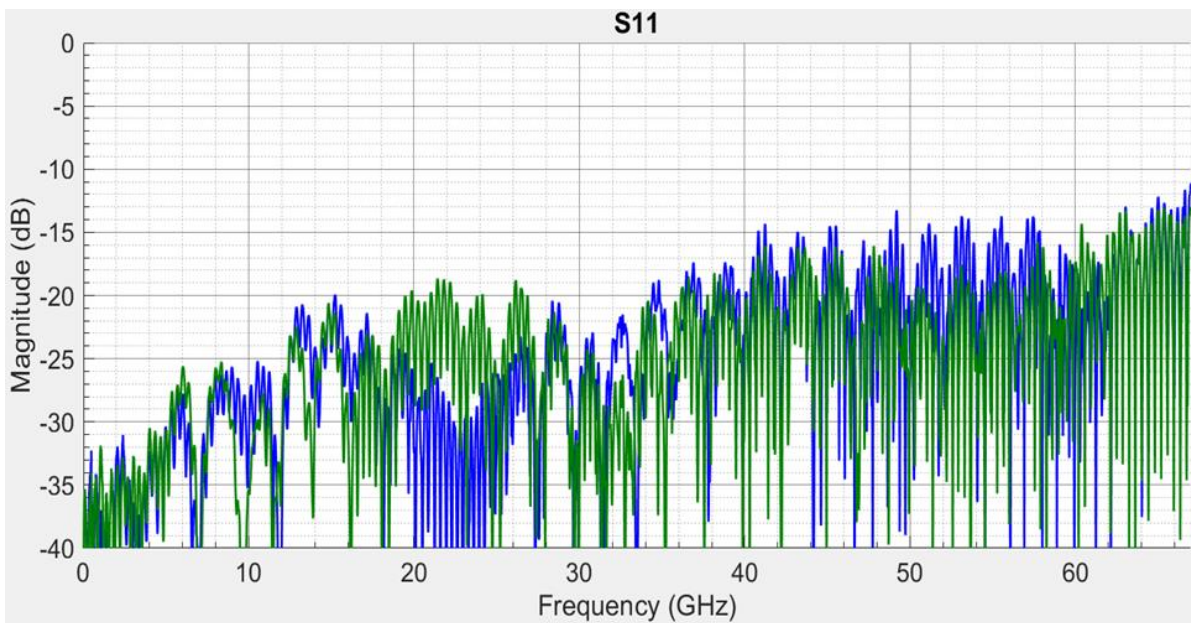


REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>8 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			



# SIGNAL INTEGRITY REPORT

## Return Loss (S11), Single-Ended (CoreHC Channels: 3, 4, Board Locations: U, V)

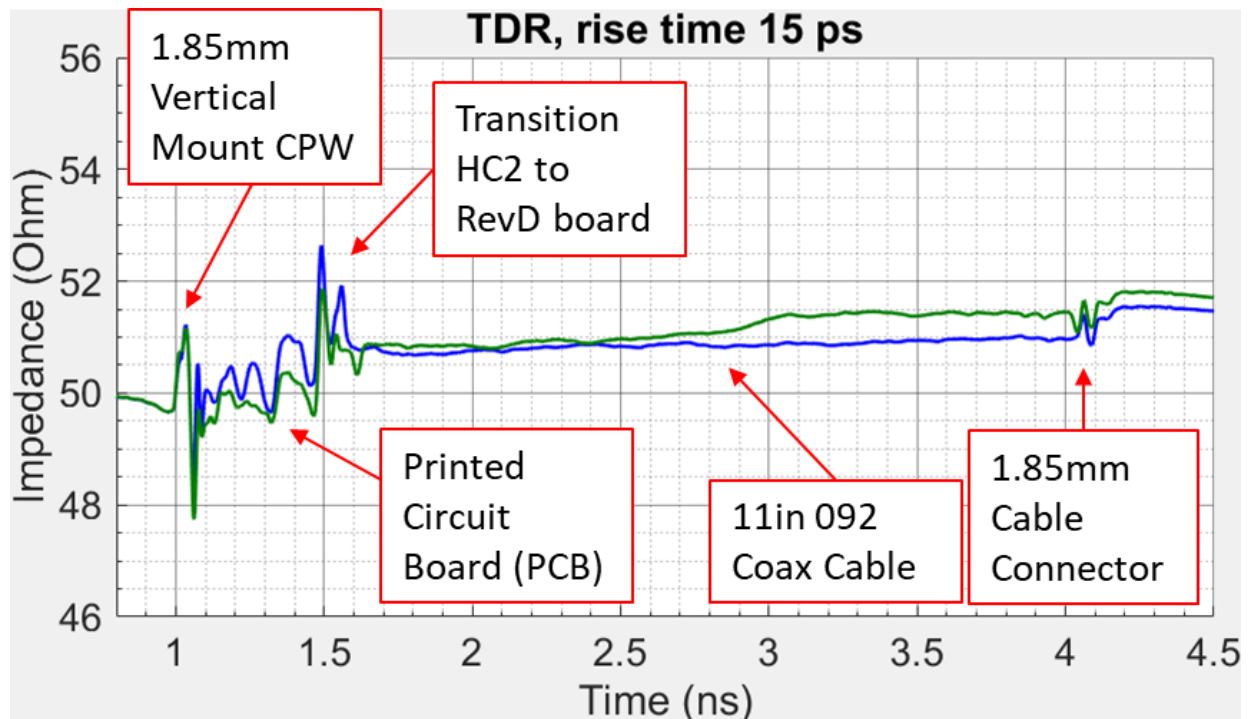
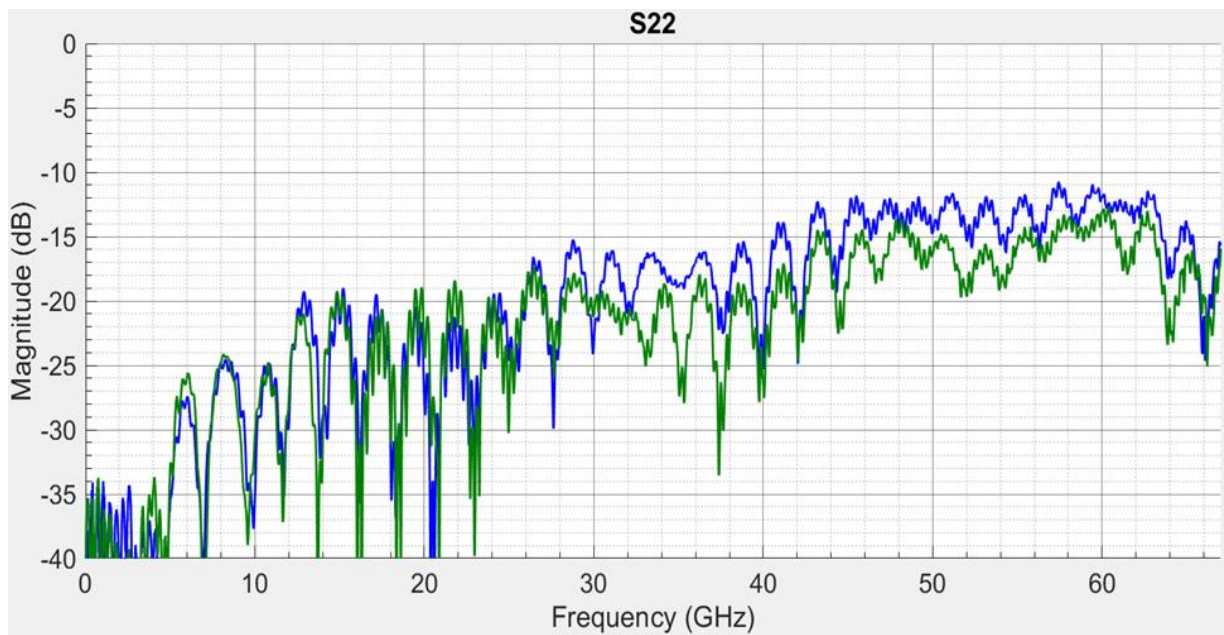


REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>9 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			

# SIGNAL INTEGRITY REPORT

## Return Loss (S22), Single-Ended

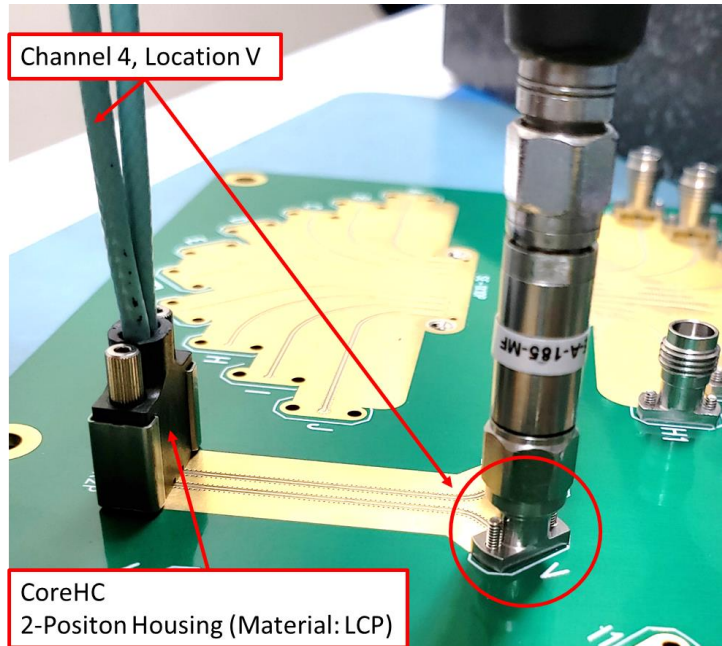
(CoreHC Channels: 3, 4, Board Locations: U, V)



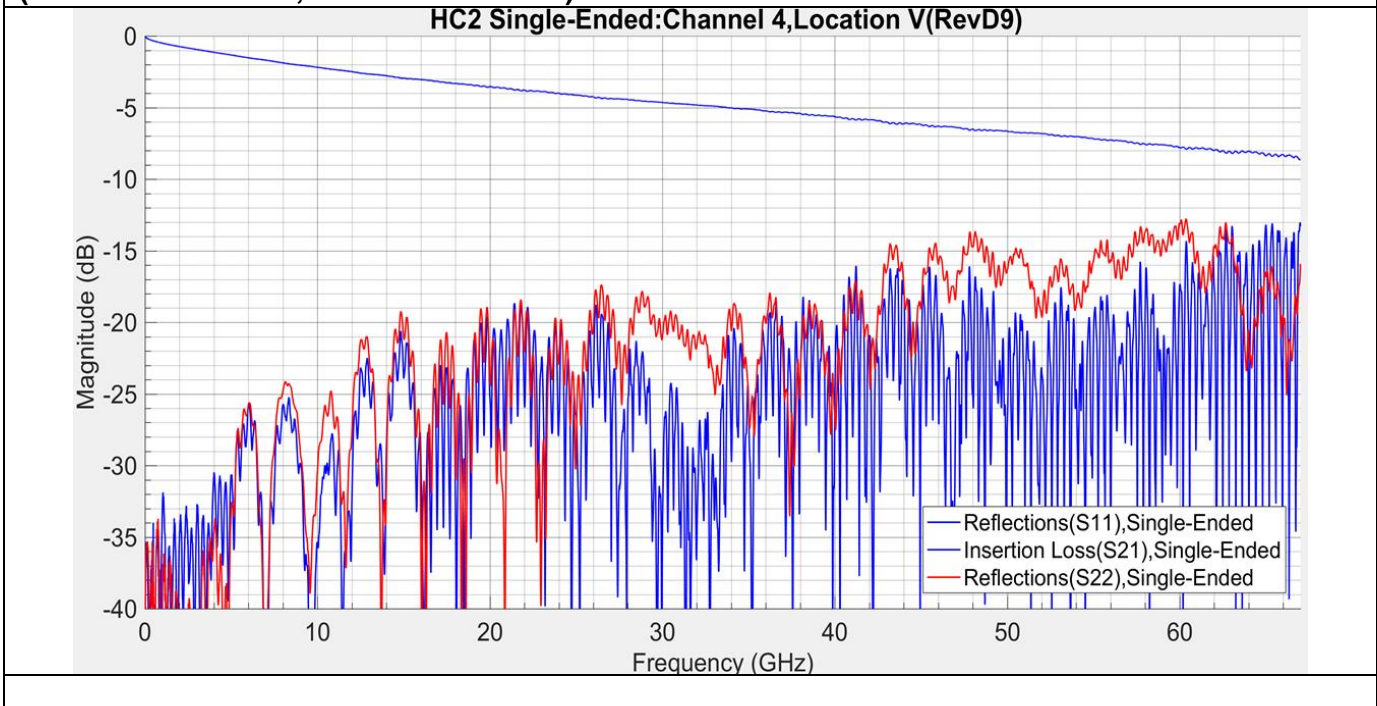
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DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			

# SIGNAL INTEGRITY REPORT

## 5.0 SIGNAL INTEGRITY RESULTS (HC2 CPW REVD BOARD), CHANNEL #4, LOCATION V



### Insertion(S21) and Return (S11, S22) Loss, Single-Ended (CoreHC Channel: 4, Board Location: V)



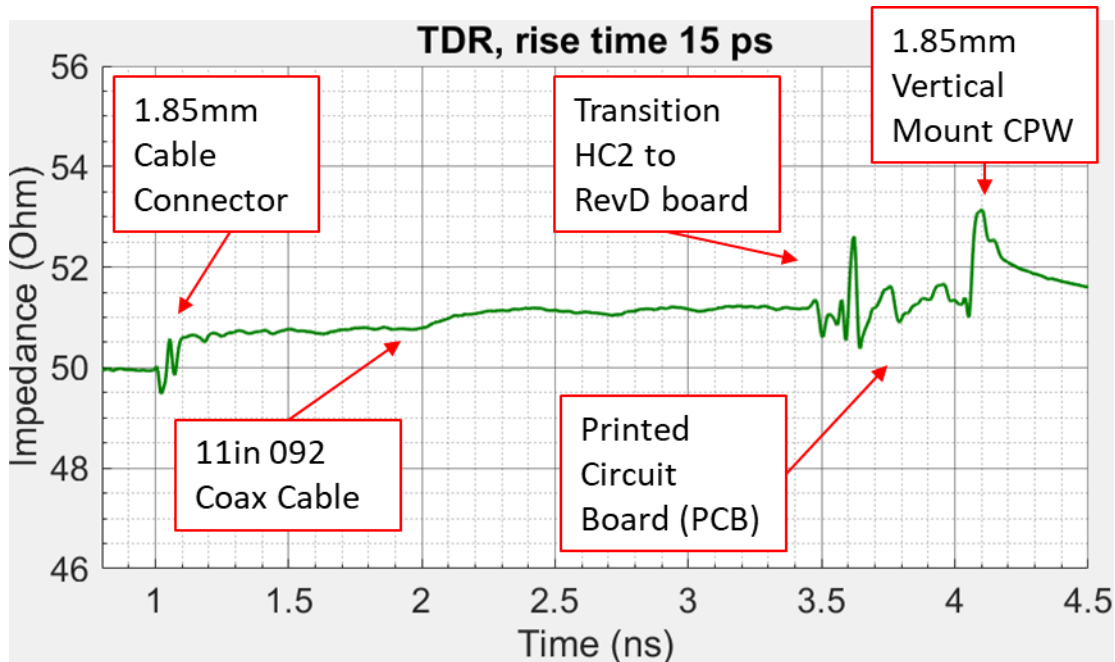
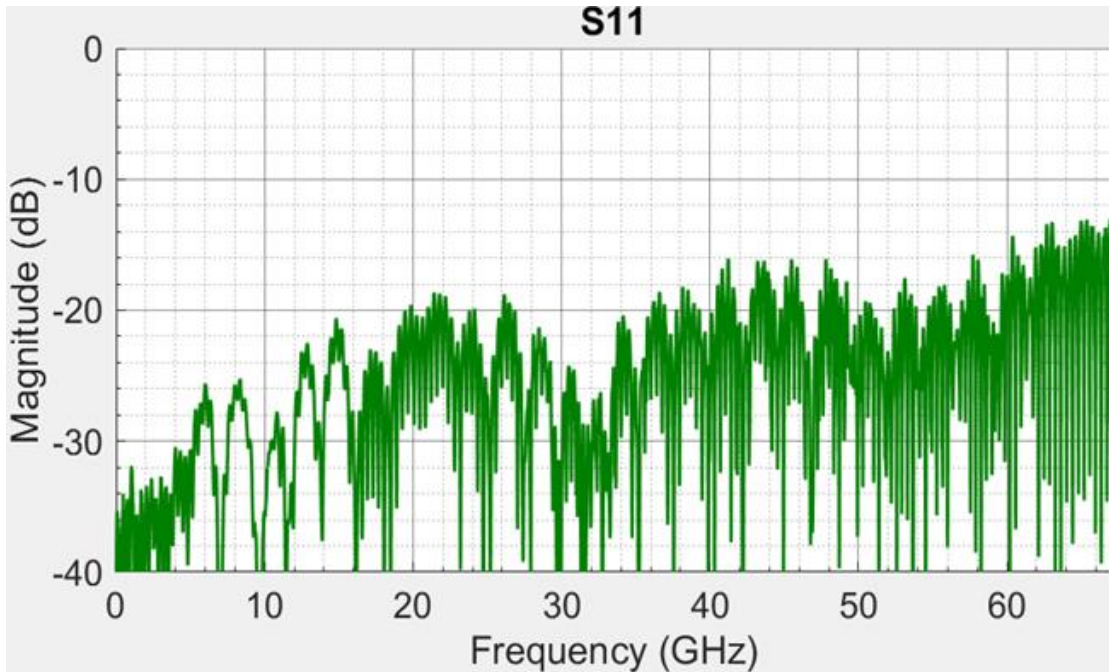
REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/ 26 / 2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>11 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			



# SIGNAL INTEGRITY REPORT

## Return Loss (S11), Single-Ended

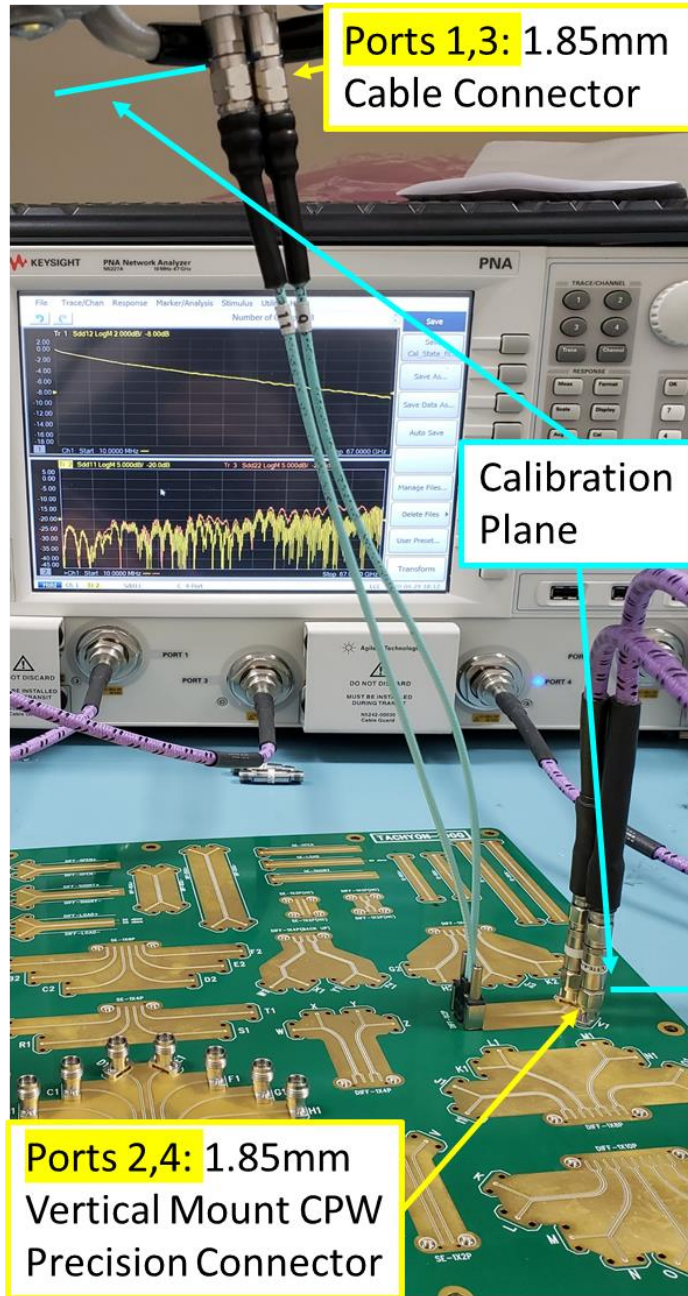
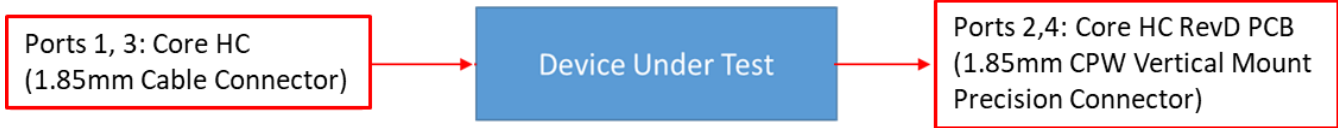
(CoreHC Channel: 4, Board Location: V)



REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>12 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			

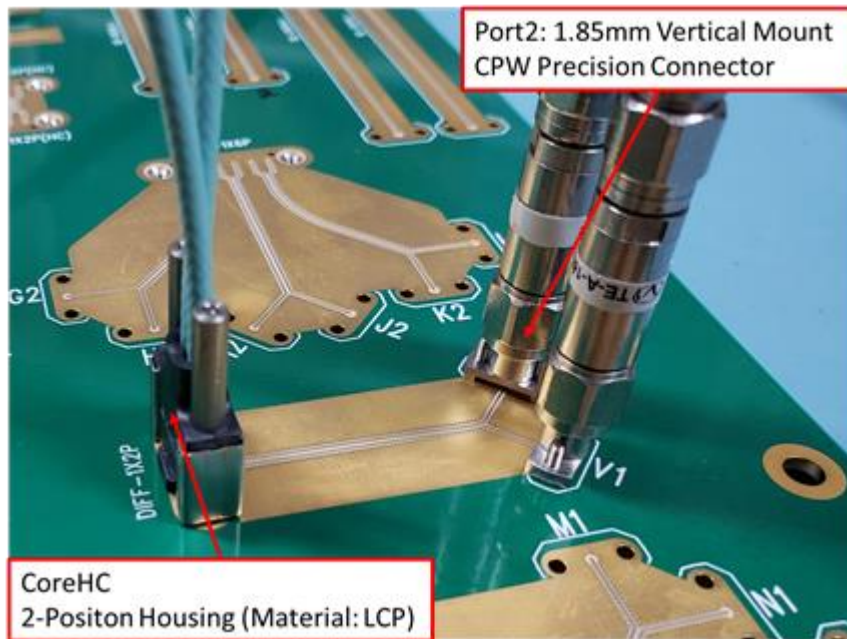
# SIGNAL INTEGRITY REPORT

## 6.0 MEASUREMENT SET-UP, DIFFERENTIAL (HC2 CPW REVD BOARD)



REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/ 26 / 2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>13 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC			

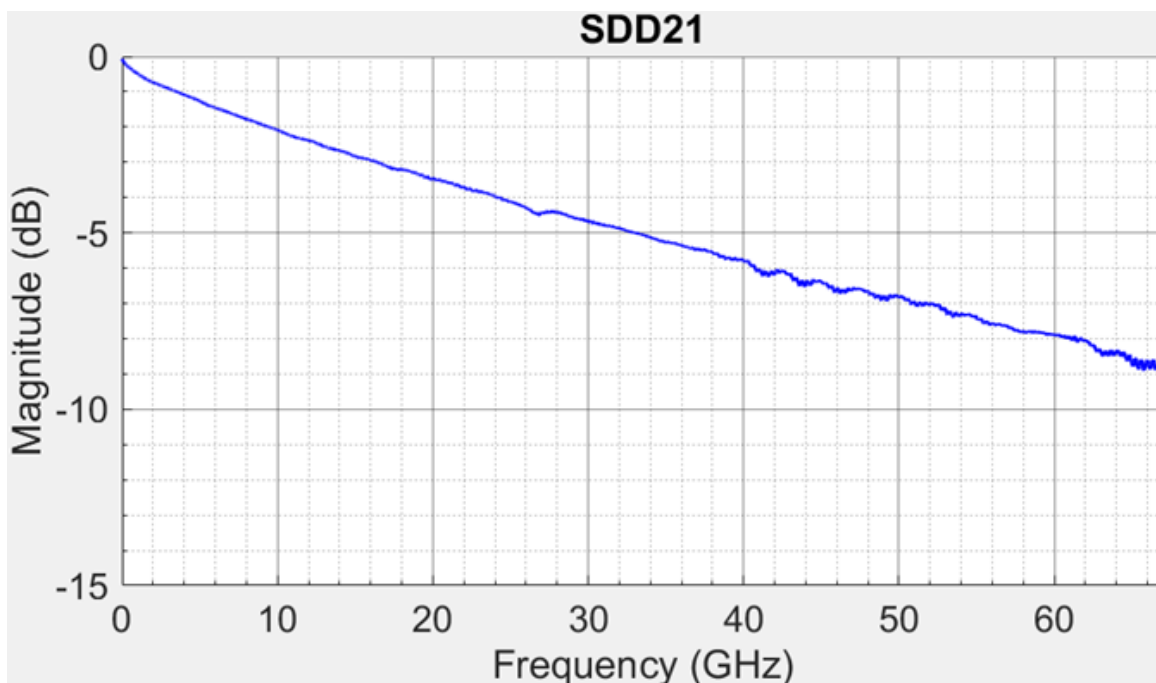
# SIGNAL INTEGRITY REPORT



## 7.0 SIGNAL INTEGRITY RESULTS, DIFFERENTIAL (HC2 CPW REVD BOARD)

### Insertion Loss (SDD21), Differential

(CoreHC Channels: 3, 4, Board Locations: U1, V1)



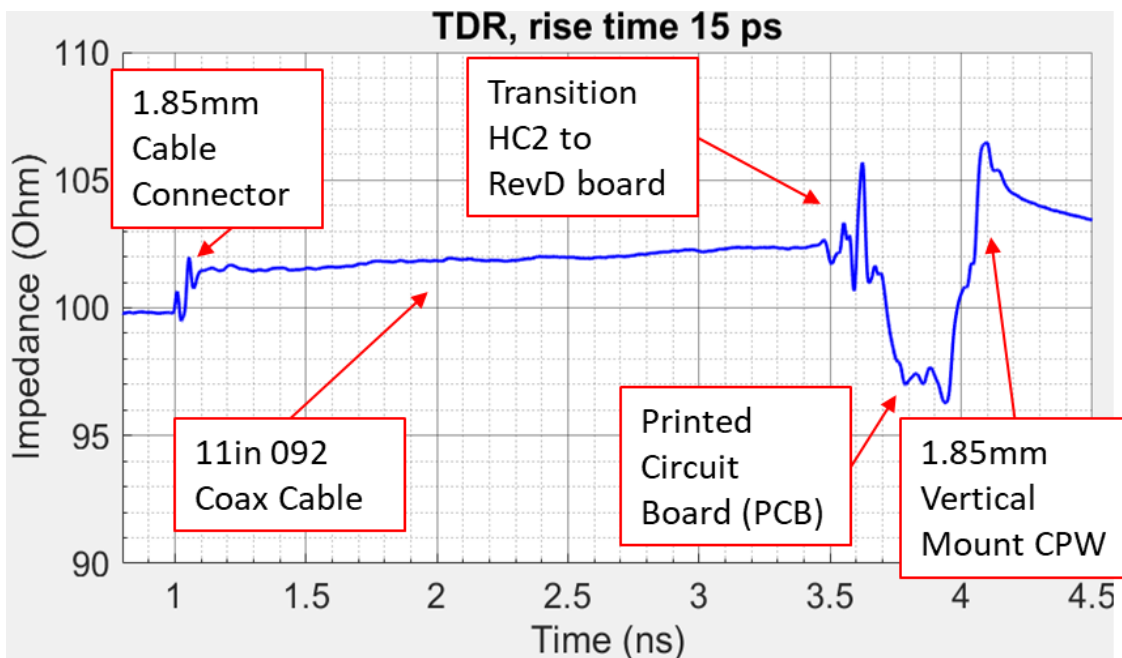
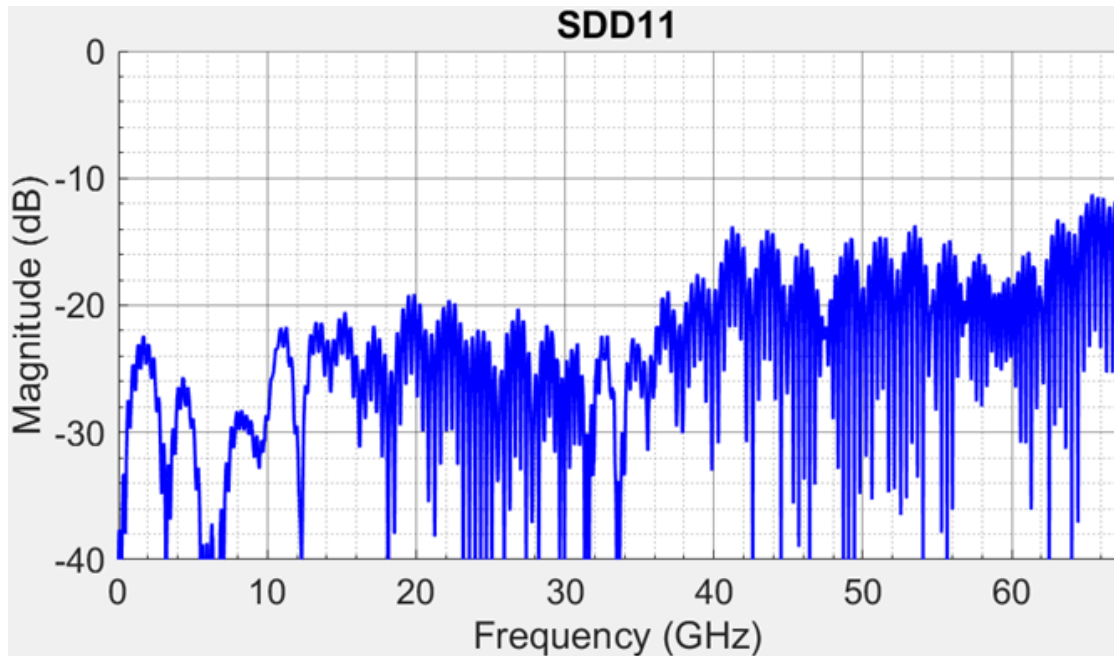
REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>14 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			



# SIGNAL INTEGRITY REPORT

## Return Loss (SDD11), Differential

(CoreHC Channels: 3, 4, Board Locations: U1, V1)

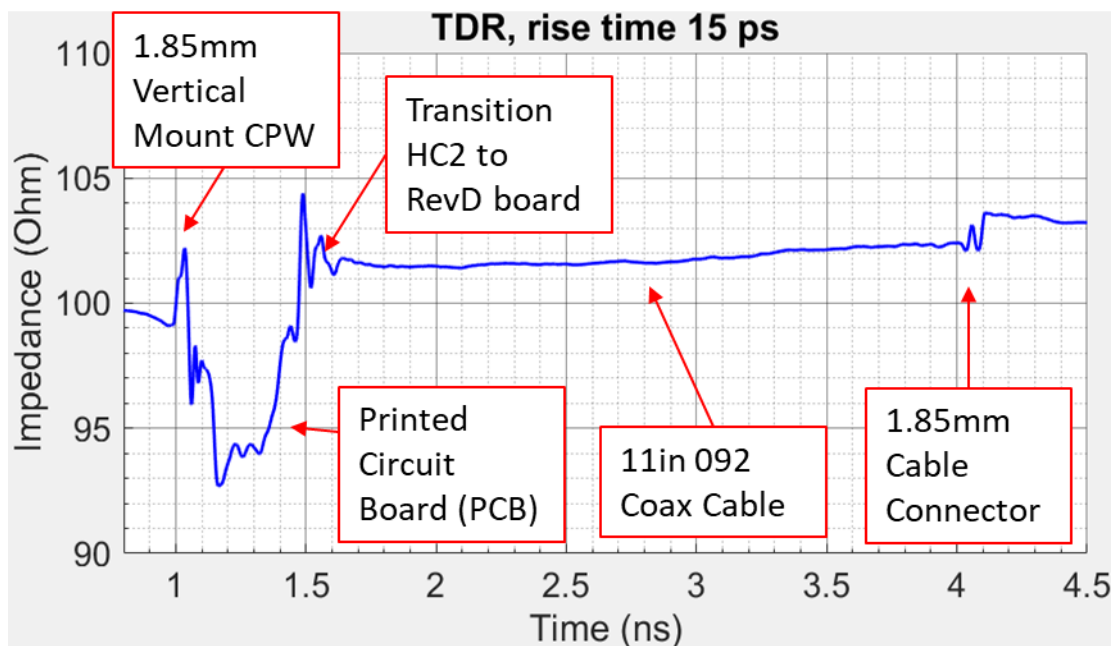
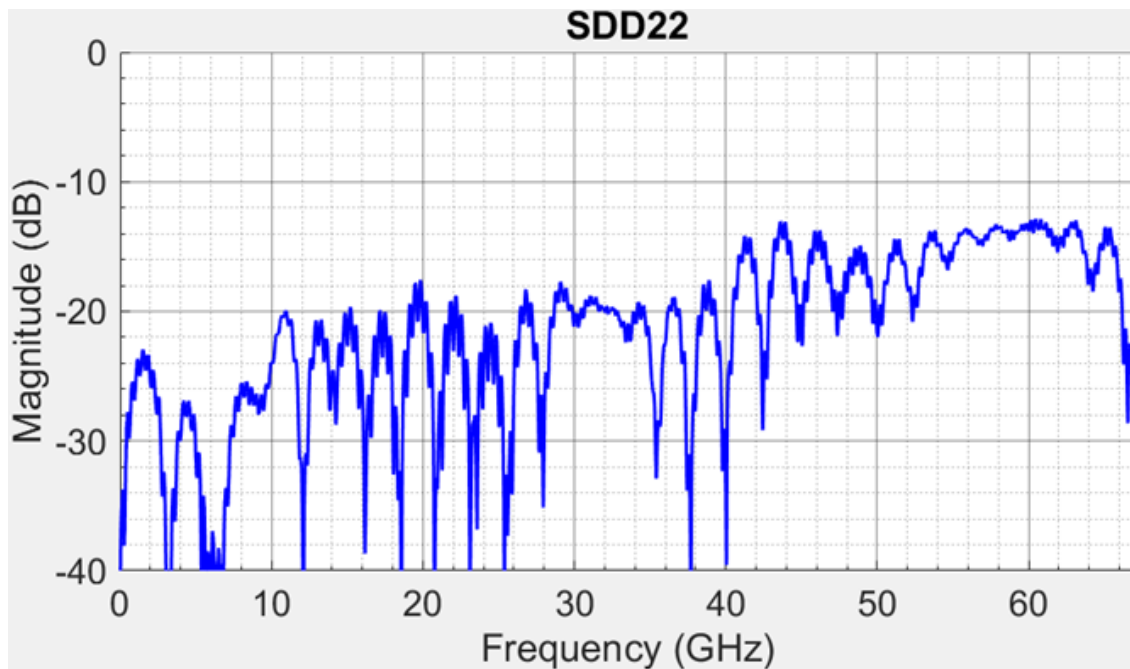


REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>15 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			

# SIGNAL INTEGRITY REPORT

## Return Loss (SDD22), Differential

(CoreHC Channels: 3, 4, Board Locations: U1, V1)

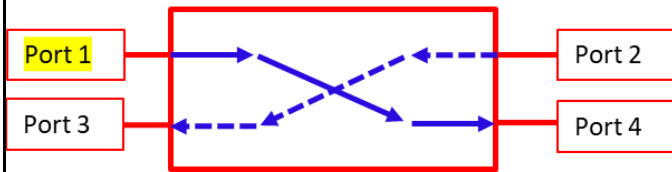


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DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			

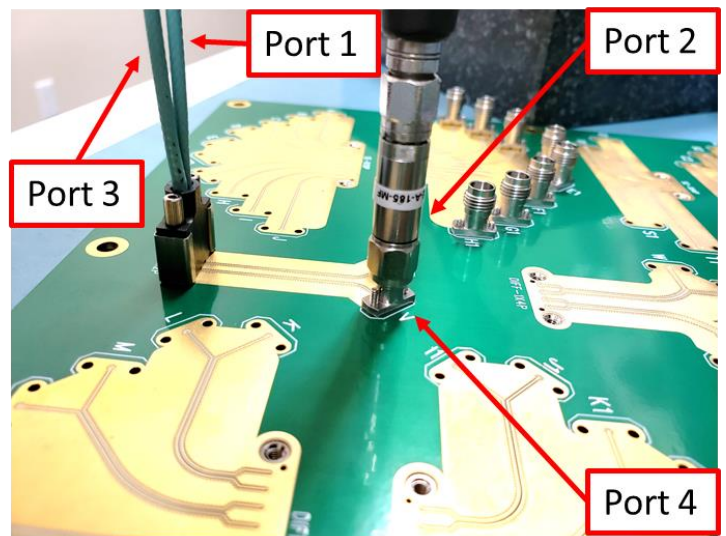
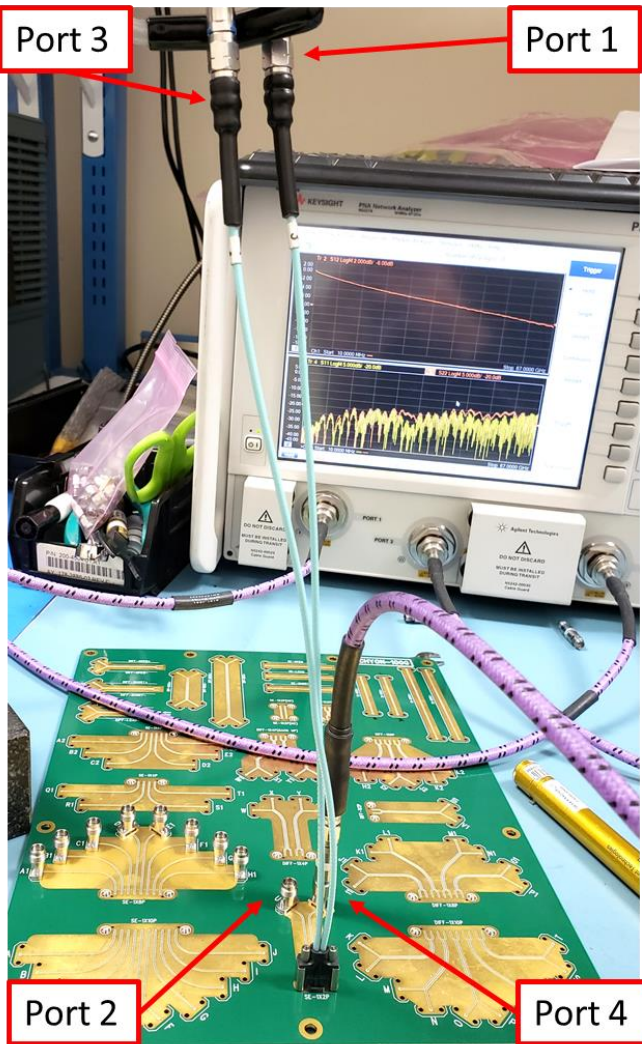
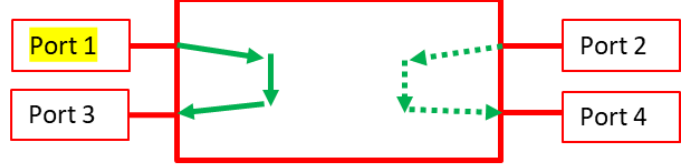
# SIGNAL INTEGRITY REPORT

## 8.0 MEASUREMENT SET-UP, SINGLE-ENDED, CROSSTALK (HC2 CPW REVD)

Far-end Crosstalk (FEXT)



Near-end Crosstalk (NEXT)



REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>17 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC			



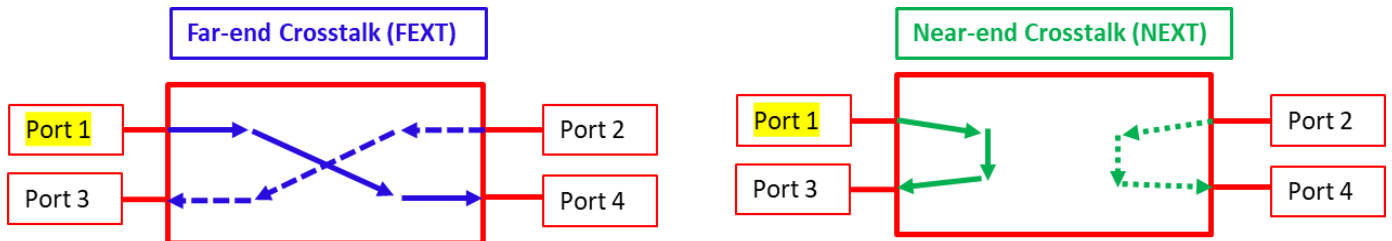
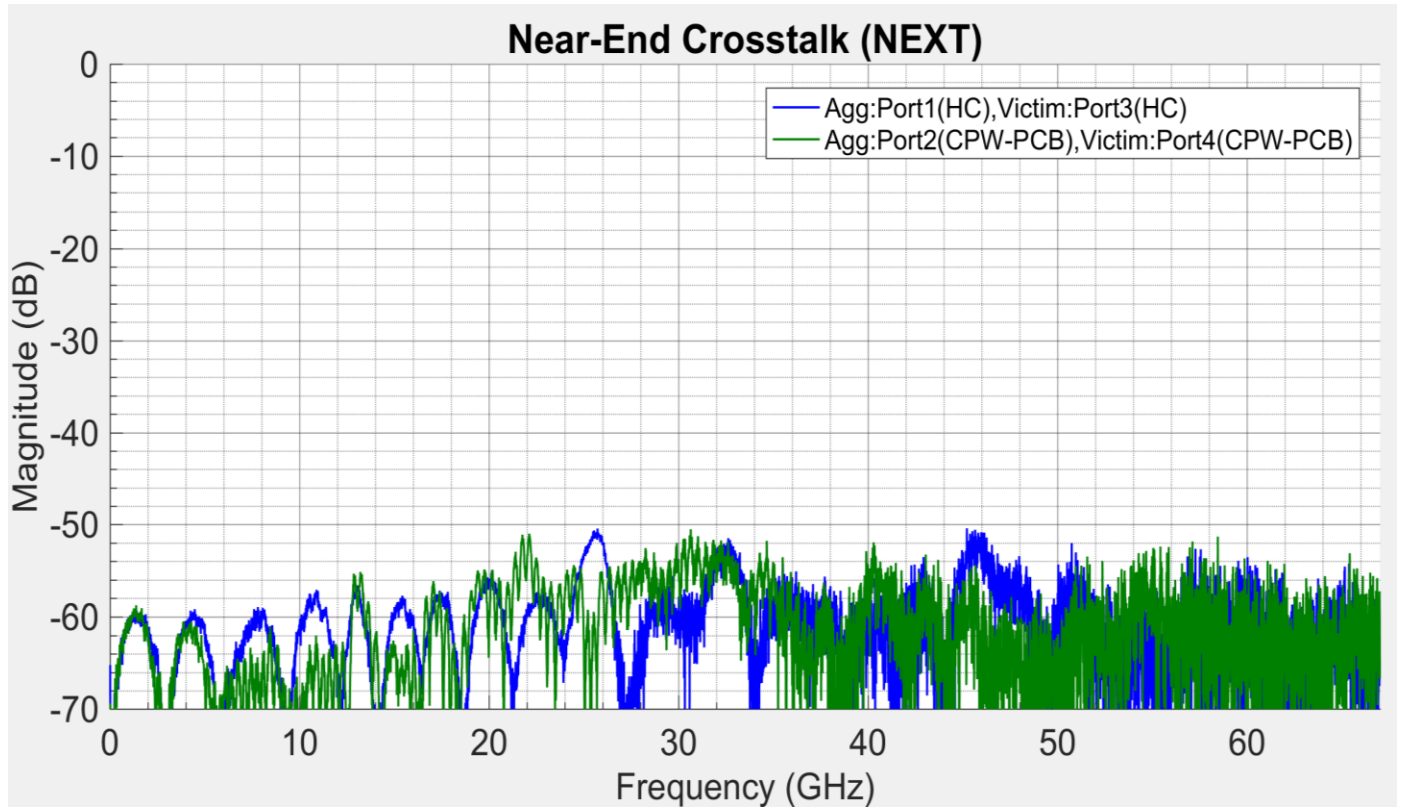
# SIGNAL INTEGRITY REPORT

## 9.0 SIGNAL INTEGRITY RESULTS, SINGLE-ENDED, CROSSTALK (HC2 CPW REVD)

### Near-End Crosstalk (S31, S42), Single-Ended

(CoreHC Channels: 3, 4, Board Locations: U, V)

Port1(HC) → Port3(HC) & Port 2(VMCPW/PCB)→ Port 4 (VMCPW/PCB)



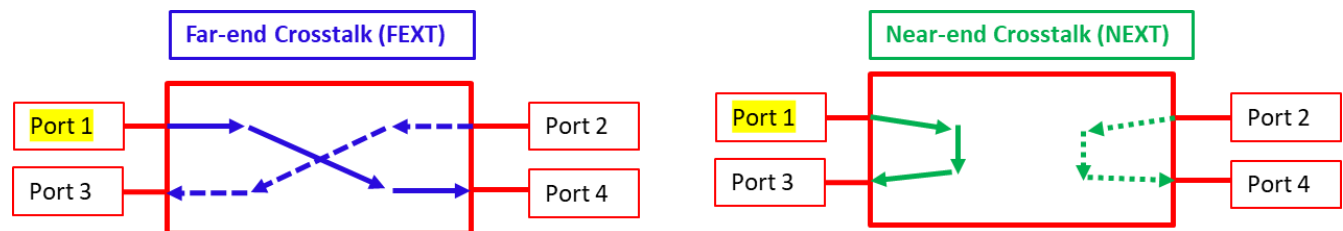
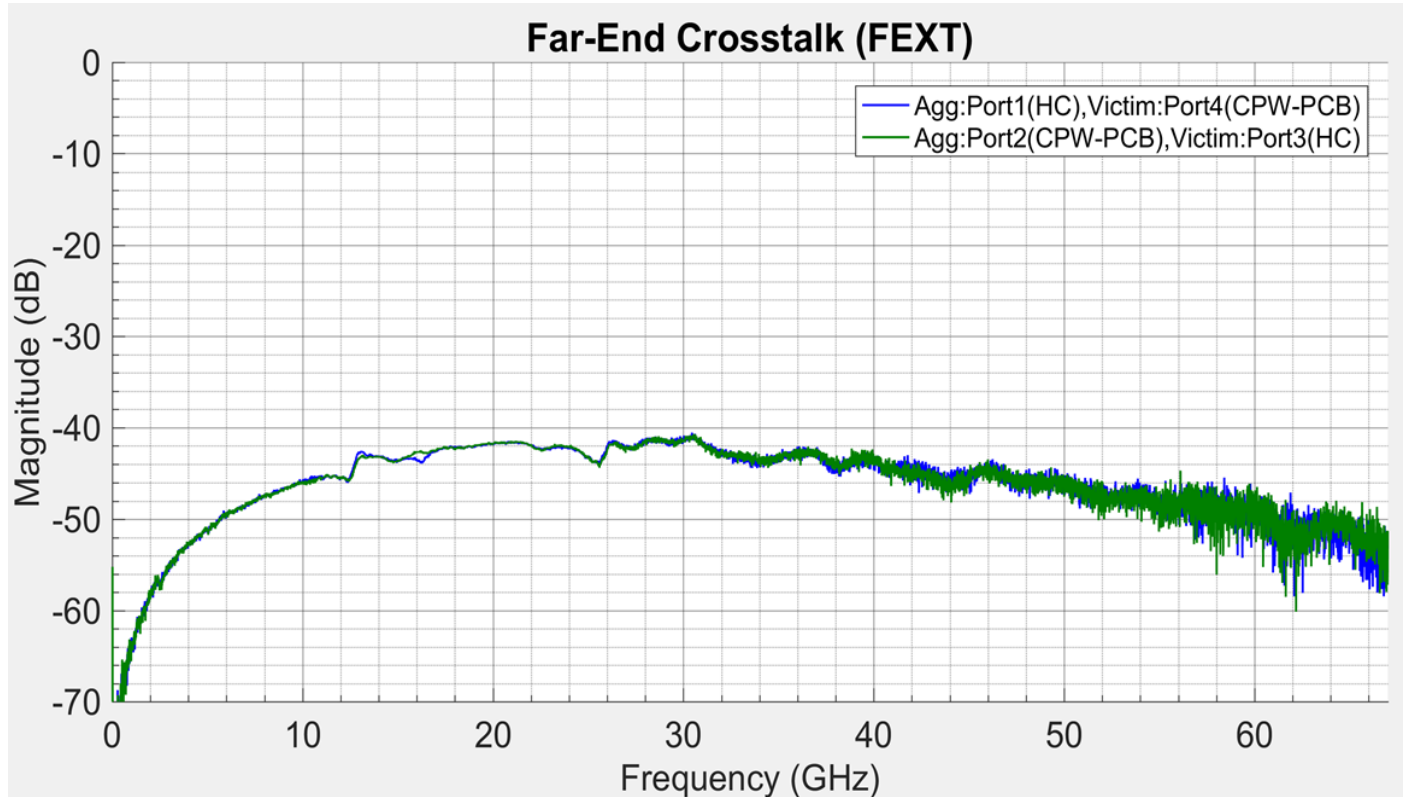
REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/ 26 / 2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>18 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			

# SIGNAL INTEGRITY REPORT

## Far-End Crosstalk (S41, S32), Single-Ended

(CoreHC Channels: 3, 4, Board Locations: U, V)

Port1(HC) → Port 4 (VMCPW/PCB) & Port 2(VMCPW/PCB) → Port3(HC)



REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>19 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			

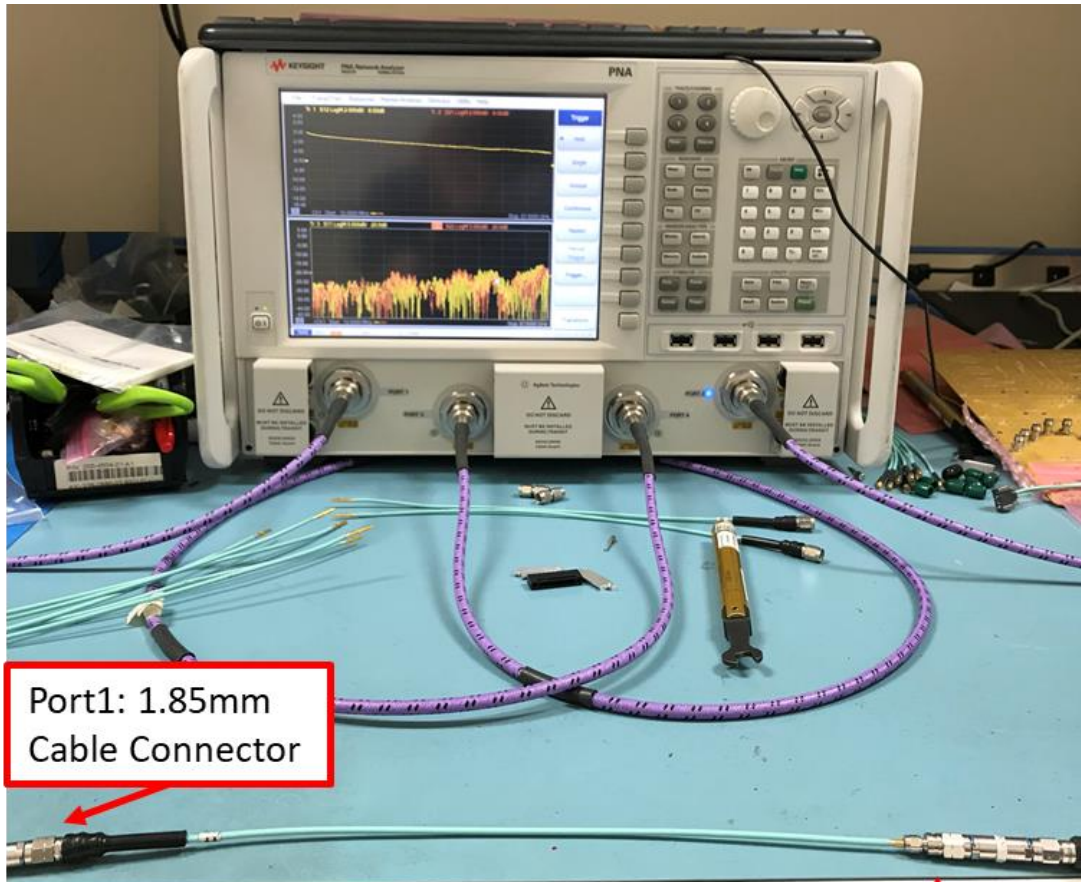
# SIGNAL INTEGRITY REPORT

## 10.0 MEASUREMENT SET-UP (HC2 1.85MM RF ADAPTOR #1)

Port 1: Core HC  
(1.85mm Cable Connector)

Device Under Test

Port 2: Core HC Interface  
(1.85mm RF Core HC Adaptor #1)



Port1: 1.85mm  
Cable Connector



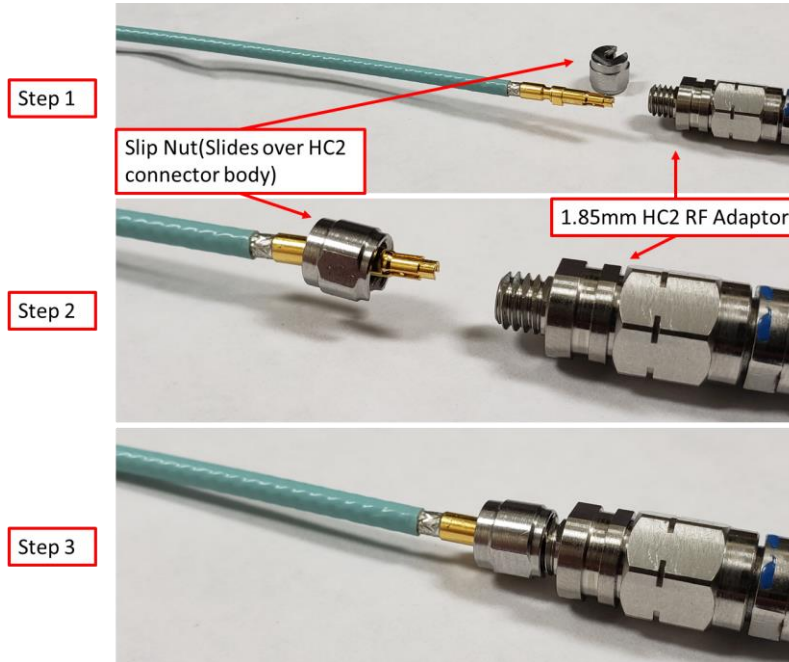
Port2: 1.85mm  
CoreHC  
Adaptor

REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/ 26 / 2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>20 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC			



# SIGNAL INTEGRITY REPORT

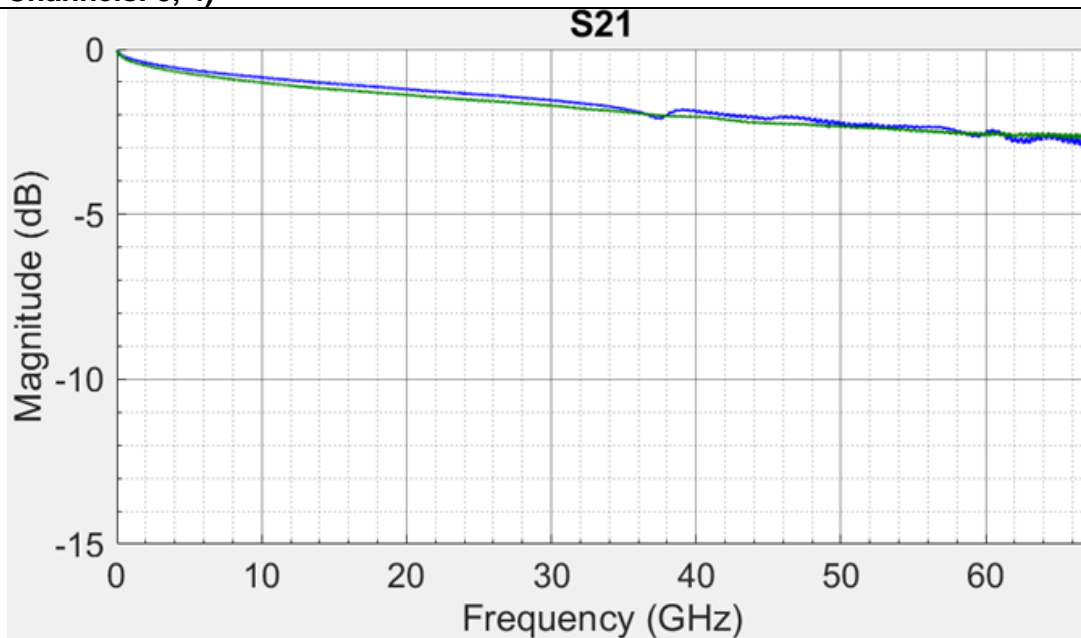
## HC2 Adaptor Testing Procedure



### 11.0 SIGNAL INTEGRITY RESULTS (HC2 1.85MM RF ADAPTOR #1)

#### Insertion Loss (S21), Single-Ended

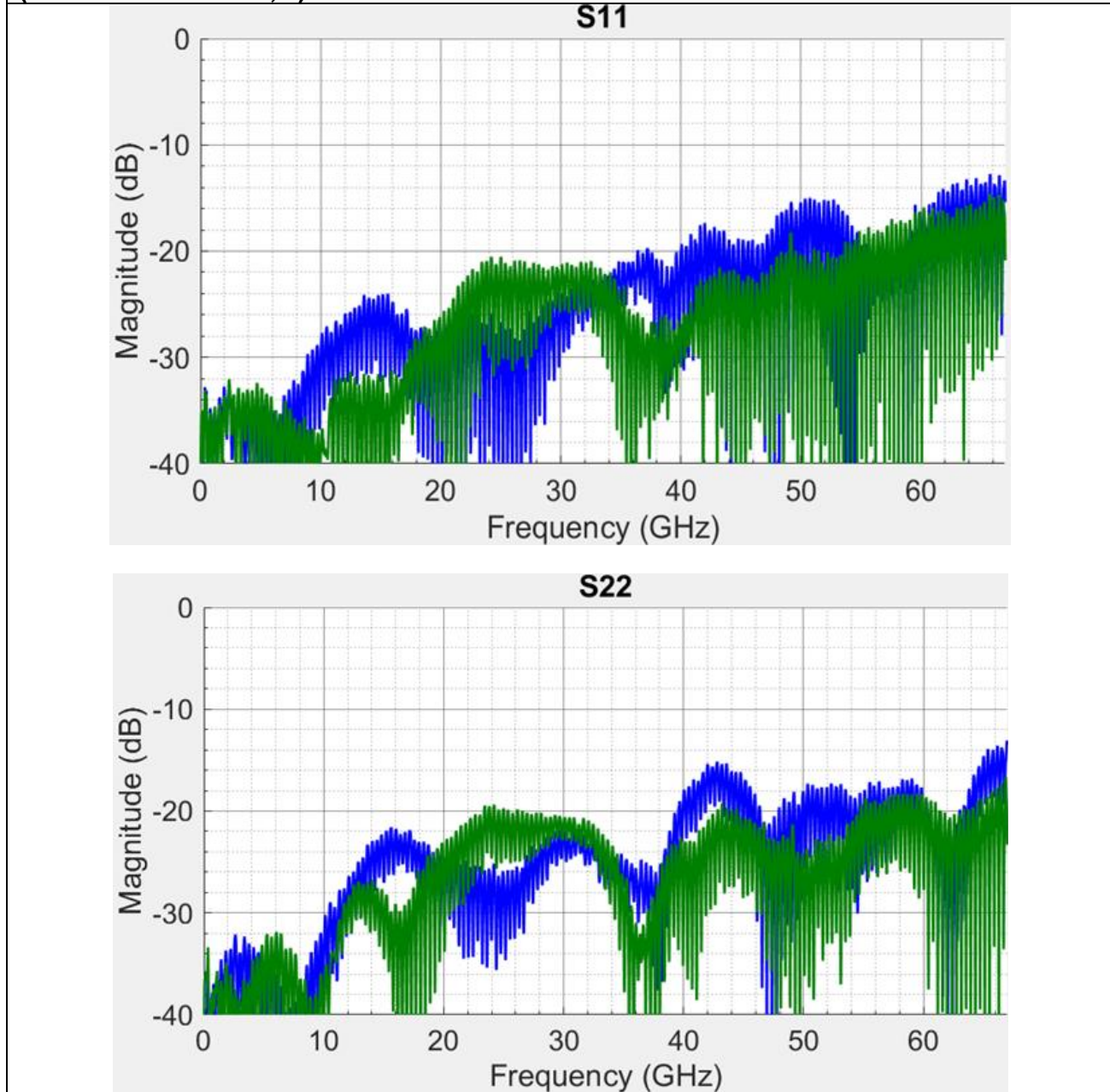
(CoreHC Channels: 3, 4)



REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>21 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			

# SIGNAL INTEGRITY REPORT

## Return Loss (S11, S22), Single-Ended (CoreHC Channels: 3, 4)



### 12.0 APPENDIX, (SPARAMETERS SHOWN IN REPORT)

CoreHC Reference Cable Assembly\_2-Position Measurements\_051420 5/14/2020 4:18 PM Compressed (zipp... 3,135 KB

REVISION: <b>1</b>	ECN INFORMATION: EC No: <b>N/A</b> DATE: <b>05/26/2020</b>	TITLE: <b>Core HC 2.5mm CPW: Configuration 1X2P (HC2 to PCB)</b> CARLISLE IT CONFIDENTIAL	SHEET No. <b>22 of 22</b>
DOCUMENT NUMBER: <b>RSI-TM7SSSH22S8MS028</b>	SI ENGINEER: <b>R.Stavoli</b>	DESIGN ENGINEER <b>H.Tran</b>	ENGINEERING MANAGER <b>E.Soubh</b>
<small>TEMPLATE FILENAME: SPM(SIZE_A)(V.1).DOC</small>			